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TEST IDEAS
Isolate your clock source
27

INSTRUMENTATION
Troubleshoot intermittent signals
37

SEMICONDUCTOR TEST
Digital signal compression in mixed-signal ATE
43

TECH TRENDS
Disciplines merge, but who pays?
19

Darryl McKenney, director of engineering services at Mercury Computer Systems.

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Page 28

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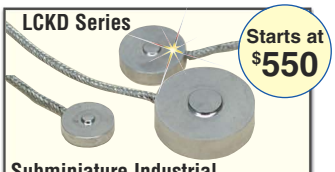

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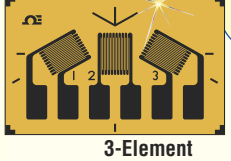

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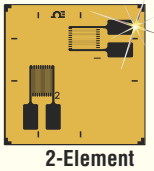

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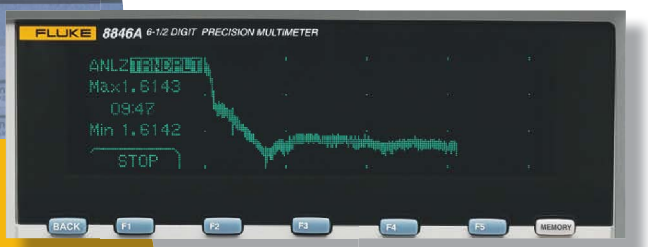

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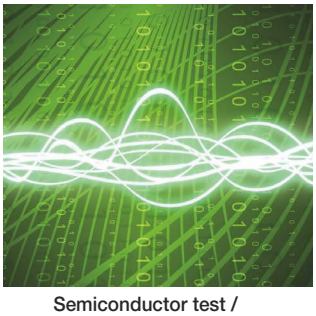
CONTENTS



Semiconductor test / Page 43

DEPARTMENTS

7 Editor's note
11 Test voices
13 News briefs
17 Show highlights:
- *Autotestcon*

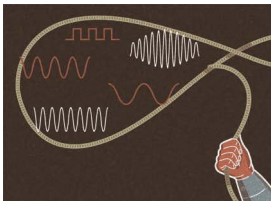
49 Product update
66 Viewpoint
8 Editorial staff
65 Business staff

FEATURES

TEST IDEAS
27 **Isolate your clock source**
Isolating a clock between an oscillator and a load minimizes noise and other interference.
By Daniele Danieli, EUROCOM-PRO, Venice, Italy

RELIABILITY TEST COVER STORY
28 **Quality by negotiation**
Engineers at Mercury Computer Systems work together to find the optimal balance among test, signal integrity, thermal analysis, mechanical fit, and component selection.
By Martin Rowe, Senior Technical Editor

INSTRUMENTATION
37 **Troubleshoot intermittent signals**
Using any of several tools and techniques on a digital oscilloscope, you can locate an elusive waveform, set up a trigger, and capture the event.
By Mike Lauterbach, LeCroy



SEMICONDUCTOR TEST
43 **Digital signal compression in mixed-signal ATE**
Compression techniques can reduce real-time waveform memory requirements or increase the performance of test instruments.
By Daniel Rosenthal, 3 dB Consulting

TECH TRENDS

19 Disciplines merge, but who pays?
21 Starting point for vision success

TEST DIGEST

23 LXI instrument classes and applications
23 Book links test and signal integrity
24 Analog effects complicate digital test

TEST REPORT SUPPLEMENT

57 **PXI Test Report**
- RF instruments challenge PXI versatility
- PXI changes how manufacturers deploy ATE
- Chassis layout is key to success with PXI Express

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Taking the Measure

Rick Nelson, Editor in Chief

- From planar transistors to 3-D microthrusters
- Body DAQ presents health, entertainment opportunities

Rowe's and Columns

Martin Rowe, Senior Technical Editor

- Should tech schools shed the nerd image?
- You know too much

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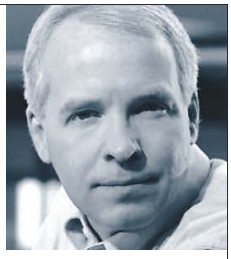

Bringing science to life through art

I've commented previously on this page (see May 2005, for example) that an engineering career isn't an easy sell to students in the US, and I applaud the efforts of organizations that are trying to instill an interest in technology in young people. Those initiatives range from the Lego WeDo platform, which adapts National Instruments' LabView graphical design environment for the grade-school set, to the US Department of Energy's EcoCar competition, which provides computer-modeling and hands-on experience for future automotive engineers. Addressing age groups in between is the FIRST program, which brings the excitement of sporting events to robotics competition.

IMEC is working to change people's perception that nanotechnology is irrelevant.

One goal of both the Lego WeDo product and the FIRST competition is to instill an interest in technology in children to open their minds to engineering careers, while EcoCar aims to enhance the skills of those who have already chosen technical fields. But a significant constituency of people—of all ages—do not and will never pursue scientific careers.

Such people, said Imke Debecker, outreach communication coordinator at the nanotechnology research center IMEC, often find scientific topics too complex to understand or simply irrelevant to their lives. She's working to change that—converting such people to "friends of nanotechnology" through IMEC outreach efforts. She hopes to instill in them the sentiment expressed by Dr. Mark Miodownik, head of the materials research group in the engineering division at King's College, London, in a BBC column titled "So who needs scientists?" "Science is like poetry," he writes, adding, "It is an expression of something sublime."

IMEC's outreach efforts address people of all ages, said Debecker, speaking at IMEC's Annual Research Review Meeting October 13 in Leuven, Belgium. For youngsters, IMEC sponsored a nanotechnology festival, where students were encouraged to describe their ultimate nanotechnology applications. My favorite: nano-camera-embedded fabric that would display on the front of clothing the view behind the wearer, rendering the wearer practically invisible.

For adults, IMEC is working with Ad!dict Creative Lab, which draws on the talents of 4000 registrants representing 32 disciplines, including fashion, photography, architecture, cooking, design, music, and advertising. Points of focus include algorithm-based emergent behavior, victimless leather grown from embryonic stem cells, biojewelry, and engineered materials. Results of the Ad!dict Creative Lab and IMEC collaboration will be highlighted in the forthcoming book *#29/in.tangible/scape.s*.

IMEC will continue its outreach program with an exhibit at the Creativity World Forum November 19–20 in Antwerp, Belgium, and the organization plans to engage 800 youngsters in nanotechnology work at the Academy of Leuven during 2009.

Participants in the IMEC outreach events may not come away with a comprehensive understanding of nanotechnology—but they might well obtain a healthy respect for the possibilities of the field. And a lack of thorough understanding might not be a bad thing, as Debecker suggested by highlighting this quote from Einstein: "The fairest thing we can experience is the mysterious. It is the fundamental emotion which stands at the cradle of true art and true science." T&MW

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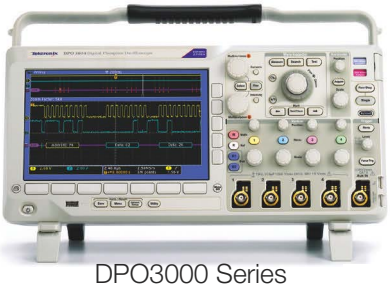

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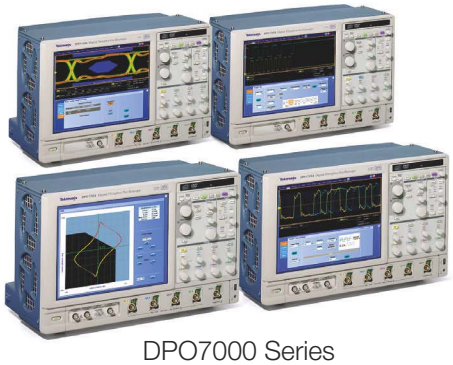

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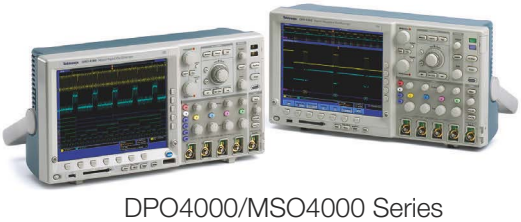

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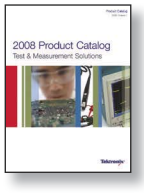

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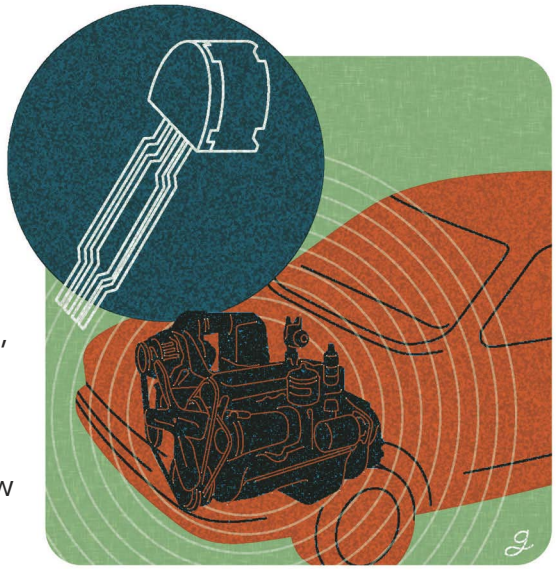

DANIEL GUIDERA

Dan Dwyer is a principal systems engineer at Allegro Microsystems in Manchester, NH, where engineers develop and test Hall-effect sensors that are used instead of mechanical switches in high-reliability applications in printers, copiers, and cellphones. Digital Hall-effect sensors are used on automobiles and motorized machines to measure rotational speed and position. Analog Hall-effect sensors sense current flow in wires. Senior technical editor Martin Rowe spoke with Dwyer by phone.

Q: What is the role of a systems engineer?
A: I assist in the development of new products from a customer and applications perspective, making sure that the product meets customer requirements. Systems engineers also provide direct technical support to large, strategically important customers.

Q: What tests do you perform to verify that products are customer ready?
A: Much of my testing involves EMC (electromagnetic compliance). Allegro doesn't have a compliance-test facility, but we need to quickly and thoroughly assess the EMC performance of our products. I test our sensors for immunity to the kinds of interference that they will encounter in the field, based on customer or market requirements. Some tests follow industry standards, while others are customer specific. We invested in an EMC test facility primarily so we'd have flexibility and complete control over our testing.

Q: Why do you perform customer-specific tests?
A: Customers, especially in the automotive industry, have tests that often vary from published standards. Each of the three major US automakers requires BCI (bulk-current injection) testing on sensors. Though all three refer to the ISO 11452-4 standard, each automaker makes exceptions to at least part of the standard and offers additional requirements.

Q: What EMC immunity tests do you perform?
A: We run radiated and conducted emissions tests. We'll subject sensors to direct RF fields using a TEM (transverse electromagnetic mode) cell. BCI, though, is the key RF test for the automotive market. The BCI test injects current into a system at frequencies from 100 kHz to 400 MHz. BCI testing is becoming popular for low-frequency product evaluations.

Q: How do you inject current into a sensor?
A: Per ISO 11452-4, I use an indirect method with a current clamp. Placing a clamp around a harness, I inject a signal into the probe that couples into the cable wiring, creating a current. With a current clamp, I can test for both common-mode and differential-mode current.

Q: How do you measure the effects of BCI on a sensor?
A: I monitor the sensor's output signal with an oscilloscope under PC control. Software controls the oscilloscope and EMC test equipment according to the parameters of the reference standard, the requirements of the DUT (device under test), and the specific customer requirements.

Q: Do you perform other customer-specific tests besides EMC?
A: In Manchester, we conduct extensive product characterization that includes both Allegro-standard and customer-specific testing. At our company headquarters in Worcester, MA, we have an environmental test lab where we perform thermal shock, temperature-humidity cycling, and HTOL (high-temperature operating life) tests. We also have a failure-analysis lab where we analyze development products and customer returns. T&MW

Every other month, we will publish an interview with an electronics engineer who has test, measurement, or inspection responsibilities. If you'd like to participate in a future column, contact Martin Rowe at mrowe@tmworld.com.

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IMEC demonstrates 3-D stacked integrated circuits

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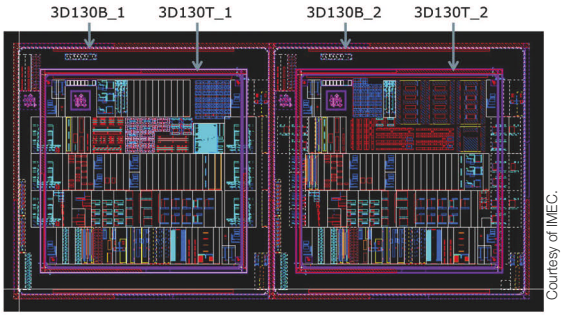

Courtesy of IMEC.

Eric Beyne, IMEC scientific director for 3-D technologies, said both the top and landing wafers contained parametric test structures for TSV characterization, CMOS ring oscillators, and other small functional circuits. Tests, he said, confirmed that the performance of the circuits does not degrade when Cu TSVs are added and the dies are stacked.

Beyne said that IMEC is ready to accept reference test circuits from its industry partners to enable them to gain early insight and experience with 3D-SIC design. IMEC plans to provide further details on its 3-D technology at a 3-D integration workshop scheduled for November 13 and 14 in Hsinchu, Taiwan. www.imec.be. (*To read our complete report about the IMEC demonstration, go to www.tmworld.com/imec_2008.*)

Spirent Communications and SGS Wireless partner on A-GPS

Spirent Communications and SGS Wireless have signed an agreement to provide validation and testing services on the Spirent ULTS (UMTS Location Test System) at the SGS Wireless laboratory in Cambridge, UK.

Under this agreement, SGS will provide Spirent with validation services to ensure that the Spirent ULTS fully supports A-GPS (Assisted-GPS) testing. In addition, SGS will use the Spirent ULTS to provide A-GPS testing services to the cellular handset industry.

SGS will provide validation services for existing PTCRB (PCS Type Certification Review Board) GCF (Global Certification Forum) certified test cases as well as for new test cases for the forthcoming OMA SUPL (Open Mobile Alliance Secure User Plane Location) Version 2.0 Enabler test specification. PTCRB certification is required for A-GPS-enabled products sold into the North American market. GCF certification is needed before many network operators outside North America will consider a product for deployment on their networks.

John Midwood, engineering manager of SGS Wireless Europe, said that SGS is "very pleased to be providing these services to Spirent Communications and the cellular industry." He added, "It enables Spirent to take advantage of the specific expertise SGS has in testing GPS enabled devices, while advancing the wireless industry's deployment of the new SUPL V2.0 standard." www.spirent.com/go/ults.

Editors' CHOICE

Simulate batteries for mobile products

Keithley's Model 2308 battery- and charger-simulating power supply lets you test and characterize battery-operated devices for their power consumption. To minimize power consumption, devices such as cellphones must change from a low-power state to full power quickly. The 2308's response to power changes can simulate how a battery responds to those current pulses.

The instrument can source voltage and sink current on either of two channels. As a battery simulator, it can maintain its output

voltage to within 90 mV in response to a pulsed current drawn by the DUT (device under test), then recover to full voltage within 35 µs. Thus, the instrument prevents false failures that might occur because of a voltage dip. The 2308 can also simulate the voltage drop caused by a battery's internal resistance, which can occur when the DUT changes from sleep to full-power mode or, in the case of a cellphone, when it transmits.

The built-in DMM (digital multimeter) can measure current and voltage drawn by the DUT. The ability to sink current lets the instrument simulate a discharged battery, which lets you test the device's battery-charging circuits. Using an integrating ADC (analog-to-digital converter), the DMM measures load current on pulsed current as short as 50 µs. Current measurement resolution ranges from 100 nA to 100 µA. The instrument also has an analog voltage output that is proportional to a DUT's load current; you can use the analog voltage with an oscilloscope to view the load current.

Price: $2795. *Keithley Instruments, www.keithley.com.*

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MCC announces burn-in system orders

Micro Control Company (MCC) has announced that it has received orders for its HPB-5B and LC-1 burn-in-with-test systems.

ISE Labs has purchased an HPB-5B system that features active thermal control for high-power semiconductor devices rated up to 150 W. The HPB-5B features individual pattern zones per burn-in board with individual temperature control for up to 48 devices, allowing device types to be mixed within the oven.

By controlling the temperature of each device, the HPB-5B manages the wide variations in heat dissipation and the diverse burn-in needs that can occur with high-power VLSI devices during the burn-in process. Memory devices can be burned-in with or without individual temperature control.

MCC also said that a Korean company has placed a $1 million order for an LC-1 burn-in-during-test system. The LC-1 can adapt to third-party vendors' burn-in boards that measure 24x12.5 in. www.microcontrol.com; www.iselabs.com.

CALENDAR

OFCNFOEC, March 22–26, San Diego, CA. Managed by the Optical Society of America. www.ofcnfoec.org.

Measurement Science Conference, March 23–27, Anaheim, CA. Sponsored by Measurement Science Conference. www.msc-conf.com.

APEX, March 31–April 2, Las Vegas, NV. Sponsored by IPC. www.goipcshows.org.

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

SignalVu analyzes 20-GHz RF signals

Editors' CHOICE

Tektronix's SignalVu vector-signal-analysis software for the DPO7000 and DPO/DSA70000 digital oscilloscope series enables engineers to characterize wideband and microwave spectral events. SignalVu combines the signal-analysis engine of the RSA6100A real-time spectrum analyzer with the triggering capabilities of the DPO7000 and DPO/DSA70000 oscilloscopes to enable designers to evaluate complex signals up to 20 GHz without using an external downconverter.

SignalVu controls all scope acquisition parameters such as record length, vertical scaling, and sample rate. The Pinpoint trigger system within the DPO7000 and DPO/DSA70000 oscilloscopes allows selection transition, state, time, or logic-qualified trigger events on both A and B trigger inputs. When a trigger event occurs, SignalVu processes the acquisition for analysis in multiple domains. All signals in an acquisition bandwidth are recorded into the scope's deep memory. Up to four channels can be captured simultaneously, and each can be independently analyzed by SignalVu software.

SignalVu uses the analysis capabilities found in the RSA6100A analyzer. In addition to providing spectrum analysis, the software can generate spectrograms that display frequency and amplitude changes over time. Time-correlated measurements can be made across the frequency, phase, amplitude, and modulation domains.

Base price: $3490 to $6990, depending on oscilloscope bandwidth; wideband radar option—$6420; wideband-communications option—$5450. *Tektronix, www.tektronix.com.*

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MIL/aerospace show highlights test systems and software

> > > Autotestcon, September 8–11, 2008, Salt Lake City, UT, www.autotestcon.com.

Intellitech introduced its Mercury Remote Diagnostic Manager (MRDM) for production or burn-in test. The software increases tester throughput by enabling the company's PT100 and PT100Pro testers to perform back-to-back testing without the need to stop to perform diagnostics on failing UUTs (units under test).

Phase Matrix officially introduced its family of PXI RF/microwave downconverter modules. The company announced at Autotestcon 2006 that it was working on the downconverter development project with **BAE Systems** and **National Instruments.** The module family consists of five PXI (3U) modules that can be configured into any one of six primary configurations operating over the frequency range of 100 kHz to 2.9 GHz, 2.7 GHz to 26.5 GHz, and 100 kHz to 26.5 GHz. The modules include an RF input conditioner module, a microwave-band input module, a low-band input module, a local oscillator module, and an IF output conditioner module.

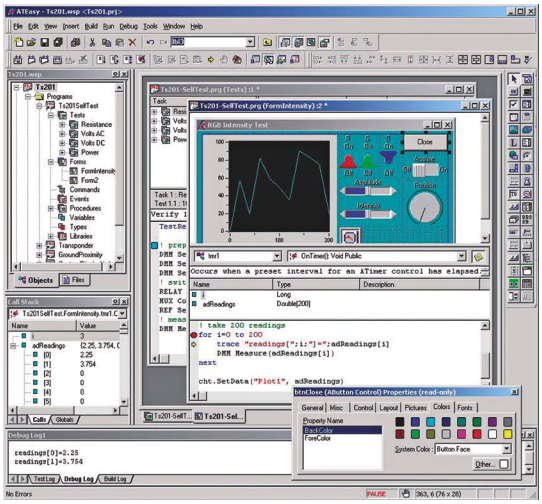
Also announcing an official debut of a product was **Huntron**, which in conjunction with **Test Evolution** (TEV) demonstrated an automated near-field signature-analysis system that combines the Huntron Access robotic probing station, Huntron workstation software, and TEV's noncontact RF near-field probe technology. Huntron demonstrated the capability in conjunction with **Metrikos** (which was subsequently acquired by TEV) at Autotestcon 2007.

Geotest—Marvin Test Systems highlighted release 7 of its ATEasy test-development software and test executive. ATEasy 7.0 features several enhancements to the test-development, run-time, and test-executive environments, including the ability to create libraries for use with external languages or by ATEasy drivers, enhanced debugging tools for the development of multithreaded test applications, and test-executive support for external test-executable programs.

Adlink Technology introduced a RoHS-compliant 3U 19-slot PXI chassis, the PXIS-2719, which provides one system controller slot, 18 peripheral card slots, a high-performance cooling design, and smart chassis management. This rack-mount-capable chassis can serve in high-capacity bench and rack-mount test-and-measurement applications.

Global Test Solutions (GTS) highlighted the line-up of instrument makers it represents, including **Bustec**, which designs and manufactures a line of VXI products. GTS said **Toellner Electronic Instruments** had signed an exclusive US distribution agreement under which GTS will distribute all of Toellner's instrumentation products in the US, including programmable DC power supplies, amplifiers, and waveform generators. GTS also announced it has signed a US distribution agreement with **Satori Technology**, which develops USB-based RF sensors. Also, a representative of **Aster Technologies** was on hand at the GTS booth to describe Aster's board-level testability analysis tools.

Also at Autotestcon 2008, **Averna** demonstrated its Universal Receiver Tester, which supports in-vehicle recording and playback to enable receiver test. **Seica** promoted the reverse-engineering capabilities of its Pilot line of flying probers. **Bird Technologies** highlighted new power-meter options for its SignalHawk portable spectrum analyzers. **GaGe** exhibited its new BASE-8 CompuScope digitizer designed for OEM customers who require analog-to-digital conversion in their systems. **KineticSystems** highlighted its new family of P216/210/206/205 cards, which are simultaneous-sampling multifunction PXI modules that provide four differential analog input channels, 14/16-bit analog-to-digital resolution, and simultaneous sampling of up to 2 Msample/s. T&MW



Enhancements to ATEasy Version 7.0 include support for ATML (automatic test markup language) test results and test descriptions as well as support for the USB interface.
Courtesy of Geotest.

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EDITOR IN CHIEF
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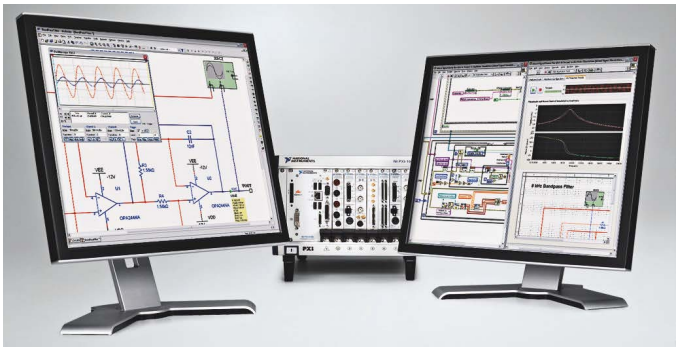
Disciplines merge, but who pays?

This final "Design, Test & Yield" column of 2008 presents an opportunity to address the interactions of these three fields throughout the year and to suggest trends that will evolve in 2009.

First, design and test grow ever closer together. Exemplifying that trend is National Instruments (NI). Mike Santori, business and technology fellow at NI, said last summer, "Over the last few years, we've begun to talk about ourselves as a design company…. NI products are now used by engineers and scientists to implement systems embedded in the product that they are trying to develop" (Ref. 1).

NI's latest effort in the blending of design and test is its October announcement of a beta version of a connectivity toolkit for the NI Multisim and LabView platforms (**figure**) that bridges the gap between design and test to reduce design errors and iterations.



A beta connectivity toolkit links Multisim and LabView. Courtesy of National Instruments.

With design and test edging closer together, instruments are getting designed into chips (Ref. 2). Although EDA vendor Synopsys offers some on-chip instrumentation functionality (see p. 24), on-chip instrument implementations remain primarily the domain of chip makers. Peter L. Levin, founder, president, and CEO of Dafca, one independent supplier of on-chip instrument technology, told me last month that "You would think on-chip instrumentation would be an emerging part of the EDA segment," but that—at least for now—this is not the case. (For more on Dafca, see the forthcoming *EDN Global Innovators 2008*, to be published later this month.)

As for yield, Phil Burlison, a director of advanced technology at Verigy who came to the company when it purchased Inovys in January, said tools can analyze and convert test-failure data into indicators of design and process problems. But the emergence of such tools poses the question: Who pays for them? An International Test Conference panel organized by Burlison was to address that question in October. I'll report on the panel online at www.tmworld.com. But it's safe to assume that the question of who pays will continue throughout 2009. T&MW

Boundary-scan test coverage for DIMM240 interfaces

Goepel electronic has introduced the CION Module/DIMM240 boundary-scan I/O module, which enables the testing of all signal and voltage-supply pins of JEDEC-standard-compliant DIMM240 sockets for DDR2-SDRAM. An onboard CION ASIC controls test execution. The new module is compatible with all Goepel ScanBooster and ScanFlex JTAG controllers and with the company's System Cascon software. www.goepel.com.

SiTest Solutions standardizes on Verigy V5000e

Verigy has announced that SiTest Solutions, a test-engineering service provider, has selected Verigy's V5000e as its test platform for flash memory. The V5000e will permit SiTest Solutions to add NAND flash and specialty-memory testing to its list of capabilities. Verigy reports that SiTest Solutions has already used the V5000e to develop a test application for a solid-state-drive device featuring integrated NAND flash memory and a memory controller in one package. www.verigy.com; www.sitestsolutions.com.

Corelis integrates functional emulation

Corelis has announced that the latest version of its ScanExpress boundary-scan tool suite, Version 6.6, combines ScanExpress JET (JTAG Emulation Test) with ScanExpress TPG test-development and ScanExpress Runner test-execution software. The new release supports full-speed functional verification without requiring modifications to the unit under test or its onboard firmware. Corelis said the new release supports its sister company Blackhawk's JTAG emulators for digital signal processors from Texas Instruments. www.blackhawk-dsp.com; www.corelis.com.

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2. Wilson, Ron, "As SOCs grow, test-and-measurement instruments move on-chip," *EDN*, February 21, 2008. www.edn.com.

USB Data Acquisition.
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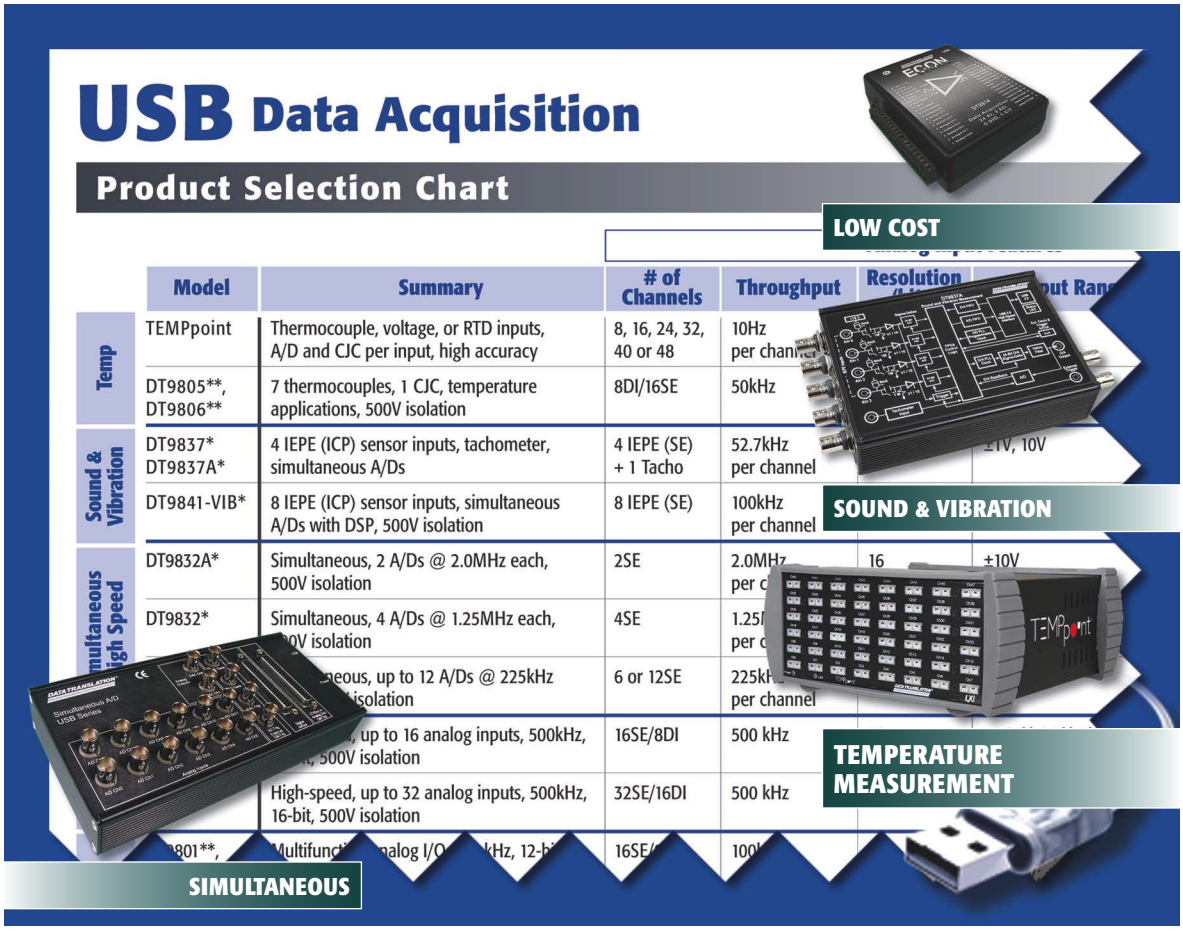

	Model	Summary	# of Channels	Throughput	Resolution	Input Range
Temp	TEMPpoint	Thermocouple, voltage, or RTD inputs, A/D and CJC per input, high accuracy	8, 16, 24, 32, 40 or 48	10Hz per channel		
Temp	DT9805**, DT9806**	7 thermocouples, 1 CJC, temperature applications, 500V isolation	8DI/16SE	50kHz		
Sound & Vibration	DT9837* DT9837A*	4 IEPE (ICP) sensor inputs, tachometer, simultaneous A/Ds	4 IEPE (SE) + 1 Tacho	52.7kHz per channel		±1V, 10V
Sound & Vibration	DT9841-VIB*	8 IEPE (ICP) sensor inputs, simultaneous A/Ds with DSP, 500V isolation	8 IEPE (SE)	100kHz per channel		
Simultaneous High Speed	DT9832A*	Simultaneous, 2 A/Ds @ 2.0MHz each, 500V isolation	2SE	2.0MHz per c	16	±10V
Simultaneous High Speed	DT9832*	Simultaneous, 4 A/Ds @ 1.25MHz each, 0V isolation	4SE	1.25M per c		
Simultaneous High Speed		neous, up to 12 A/Ds @ 225kHz isolation	6 or 12SE	225kH per channel		
Simultaneous High Speed		up to 16 analog inputs, 500kHz, 500V isolation	16SE/8DI	500 kHz		
Simultaneous High Speed		High-speed, up to 32 analog inputs, 500kHz, 16-bit, 500V isolation	32SE/16DI	500 kHz		
Simultaneous High Speed	801**,	Multifunc analog I/O kHz, 12-bi	16SE/	100		

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Starting point for vision success

If you're considering machine vision, it's tempting to get caught up in camera choices, lighting schemes, and setup programs. But you should ignore such thoughts until you have thoroughly analyzed your application, according to David Dechow, president of Aptúra Machine Vision Solutions, a Michigan integrator.

"Many vision applications fail or have only limited success because people neglected this important analysis stage," said Dechow, who has spent 25 years as an engineer, programmer, and manager in the vision field.

Dechow explained that even before this analysis begins, you need to understand what your process needs with respect to inspection, and you should also understand your company's quality requirements. How much is your company willing to spend for improved inspection? And who will be the project's champion—or will decisions be left to a committee, a far less appealing approach?

A camera checks surface quality on electronic components. You should postpone selecting components for vision systems until you've thoroughly analyzed your application, according to integrator David Dechow.
Courtesy of David Dechow.

For application analysis, Dechow uses questionnaires with his clients to probe a series of issues surrounding the current production process, inspection criteria, and part descriptions. Among many key questions: What in the production process is causing the errors? How are bad parts rejected under the current system, and what remedies have you already put in place to improve production? What features of the part need to be inspected? Do you need to read a bar code?

Dechow also is a big believer in having a thorough description of the part to be inspected. This description should involve physical details about geometric structure and features, as well as all possible part variations, including color, size, materials, and surface finish. And will the part change over time?

"The part description, including drawings and photos, is essential because your inspection system must be flexible enough to handle all possible variations," explained Dechow.

Equally important is a thorough understanding of the material-handling system that delivers the part to the inspection station. What will be the speed and throughput of the system—and the positional variations of the part? Will there be shock and vibration? Machine vision is extremely sensitive to how a part is presented, and solving that challenge can be even more difficult than designing the inspection system. Said Dechow: "The part needs to be positioned properly for the camera, and accomplishing that in a production setting is a lot harder than doing it on a flat bed in the lab."

Other key questions in application analysis involve the operator interface. Do you want the machine operator to see results of the inspection or have access to the machine-vision control system? Does the vision system need to interface with a PLC (programmable logic controller) or a robot?

Finally, the automation team must agree on what will constitute success in a new inspection system. That entails defining specific acceptance criteria for a part, a process that typically includes defining all the attributes of a good part.

It's only after you've taken these and other application analysis steps, said Dechow, that you're ready to move on to the project specification stage, where you actually design the inspection system and choose the hardware and software you'll need. T&MW

Backlight improves accuracy

Based on the same principles as telecentric measuring lenses, the Telecentric Backlight Illuminator from Edmund Optics uses parallel rays to eliminate parallax errors and improve gauging accuracy in machine-vision applications. The illuminator is compatible with the company's Silver series of telecentric measuring lenses. www.edmundoptics.com.

AOI system examines fine wires

Designed for small wire-bond analysis, the S6053BO-V AOI (automated optical inspection) system from Viscom is equipped with a universal high-resolution camera module that enables it to carry out inspections down to a resolution of 2 µm to 5 µm per pixel. The module can be arrayed with one or several cameras and specialized illumination units for inspecting bond wires smaller than 20 µm in diameter. For fast cycle times, the system is available in a dual-track configuration. www.viscom.com.

GigE: Right fit for line scan?

A white paper by Basler Vision Technologies examines the advantages of using the GigE (Gigabit Ethernet) protocol for line-scan vision applications. While there are still some speed and triggering issues to address, the paper notes that GigE allows cable lengths as long as 100 m, versus a 10-m limit for Camera Link. GigE also saves costs by eliminating converter boxes and frame grabbers. www.baslerweb.com.

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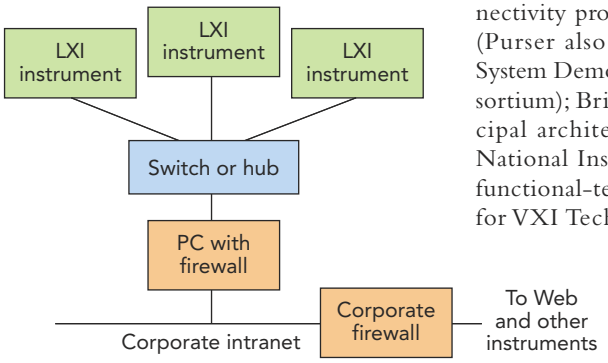
WEBCAST

LXI instrument classes and applications

Since December 2005, the LXI Consortium has acquired 52 member companies, 16 of whom are instrument vendors who have released 525 LXI-compatible instruments, reported Conrad Proft, a technology product planner/applications engineer at Agilent Technologies, during a September 10 Autotestcon presentation titled "Test Applications Using LXI Instruments." During the presentation, presented in Webcast format on September 24 in conjunction with *Test & Measurement World*, Proft and his co-presenters reviewed LXI basics, described how to put an LXI system together, and explained the three LXI instrument classes while highlighting potential applications for each.



LXI instruments can exist on an isolated subnet yet communicate with other instruments around the world.

Class C instruments represent the base class, incorporating such features as a Web browser and IVI (interchangeable virtual instrument) driver API (application programming interface), Proft said, noting that Class B instruments add synchronization capability via the IEEE 1588 precision time protocol and support peer-to-peer messaging. Class A instruments, he said, add a fast hardware trigger bus. Proft noted that LXI-based systems require only one Ethernet cable per 19-in. rack and therefore support much higher instrument densities than does GPIB.

Proft's co-presenters were Rob Purser, the senior team lead for connectivity products at The MathWorks (Purser also leads the Multi Vendor System Demo group for the LXI Consortium); Brian Powell, software principal architect in LabView R&D at National Instruments; and Tom Sarfi, functional-test business unit manager for VXI Technology. In the archived Webcast of the presentation (www.tmworld.com/webcasts), Proft explains how to set up LXI instruments on an isolated subnet (**figure**), Purser describes a 1588 time-synchronization demonstration and a far-field antenna measurement demonstration presented at Autotestcon, Powell comments on LXI software compatibility, and Sarfi describes a distributed application that employed Class A instruments to support more than 10,000 channels of strain-measurement data acquisition.

Rick Nelson, Editor in Chief

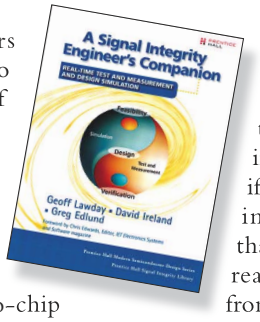
BOOK REVIEW

Book links test and signal integrity

A Signal Integrity Engineer's Companion: Real-Time Test and Measurement and Design Simulation, by Geoff Lawday, David Ireland, and Greg Edlund. Prentice Hall Pearson Education (www.prenhallprofessional.com), 2008. 460 pages. $85.50.

Signal integrity has become synonymous with high-speed serial data links, and this book strengthens the "link" between the two. In truth, the book's subtitle is more descriptive of its contents than the main title, because the bulk of the text covers test equipment, test processes, and physical-layer standards compliance.

From reading this book, you'll learn which type of test to perform on signal paths and what test equipment you'll need. This book covers oscilloscopes (both real-time and sampling), logic analyzers, probes, and signal sources that you can use to characterize a transmission channel and compare your results to simulations. The authors dedicate an entire chapter to probes—an essential part of any measurement. In fact, the book covers probes before covering oscilloscopes and logic analyzers.



The authors dedicate two chapters to case studies: one discusses the chip-to-chip communications used in DDR2, and the other discusses using PCI Express for communications between a host board and a peripheral. In both cases, the authors take you on a journey to complete a table where you verify whether a simulation has sufficient design margins. The DDR2 case study takes you through a timing analysis. You determine if a design has enough timing margin to guarantee that a system will properly read and write data to and from memory. The PCI Express exercise builds upon chapters that cover transmitter and receiver testing and asks you to complete a table on jitter analysis and signal loss. The case studies cover printed-circuit board traces, vias, and connectors and how

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Book links test and signal integrity *(continued)*

they contribute to timing and amplitude problems.

You will find some fundamental information about signal integrity in this book, but not an in-depth theory of signals, jitter, and bit-error rate, which are so tightly associated with signal integrity. In fact, the authors barely mention the different types of jitter that often appear in serial data streams. You will, though, learn about setup-and-hold issues, rise and fall timing, and circuit modeling.

This book follows a trend of using black-and-white images only in print, which doesn't work when you try to look at screen images of timing and eye diagrams. The text refers to image colors that you can't see on the printed page—to see the color, you need to buy an electronic copy of the book.

Martin Rowe, Senior Technical Editor

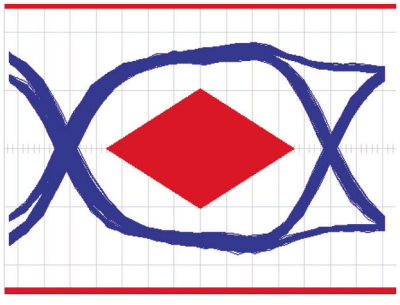
SEMICONDUCTOR TEST

Analog effects complicate digital test

The term "analog" conjures up visions of op amps and data converters, but Navraj Nandra, director of marketing for mixed-signal IP at Synopsys, explains that "The speeds of today's chips' serial digital I/O lines ensure that analog effects come into play" even in ostensibly all-digital parts. Complicating matters, he said, is that pure analog companies have the luxury of implementing functions in processes optimized for analog circuitry. In contrast, companies making digital chips want to implement their high-speed I/O in standard deep-submicron digital processes—with all the attendant process-variation and signal-integrity issues.

Synopsys addresses serial I/O design problems with its DesignWare IP to implement functions such as USB 2.0, DDR2/3 memory, SATA, and PCI Express 2.0 interfaces. The DesignWare PCI Express 2.0 product, for example, includes the physical layer interface, or PHY, running at 5 Gbps as well as a digital controller and verification IP.

Of course, IP isn't useful if it isn't testable—in the lab or on the production floor. For lab tests, Synopsys obtains split-lot samples from foundries and evaluates them using demo boards, performing eye-diagram mask tests using bench oscilloscopes (**figure**). For production test, Synopsys builds diagnostic IP into its PHYs—essentially on-chip sampling oscilloscopes accessible via a JTAG port, enabling a conventional digital tester to perform real-time eye-diagram mask testing.



An eye-diagram mask test illustrates the performance of Synopsys PHY IP for PCI Express 2.0. The diagram can be directly observed on an oscilloscope from a demo board; for production test, an internal sampling-scope function makes the eye diagram available to a standard digital ATE system via a JTAG port. Courtesy of Synopsys.

The Synopsys Website provides a video demo of a lab test of a PCI Express 2.0 PHY device. The online version of this article (www.tmworld.com/2008_11) contains a link to the demo as well as a link to my story, "Handcrafted analog gets automated assist," from the September 4 issue of sibling publication *EDN*. You'll also find a link to Nandra's August 21 *EDN* article, "On-chip test capabilities solve the analog test problem for high-speed serial interfaces," in which he provides details on automating eye-mask tests using a digital production tester.

Rick Nelson, Editor-in-Chief

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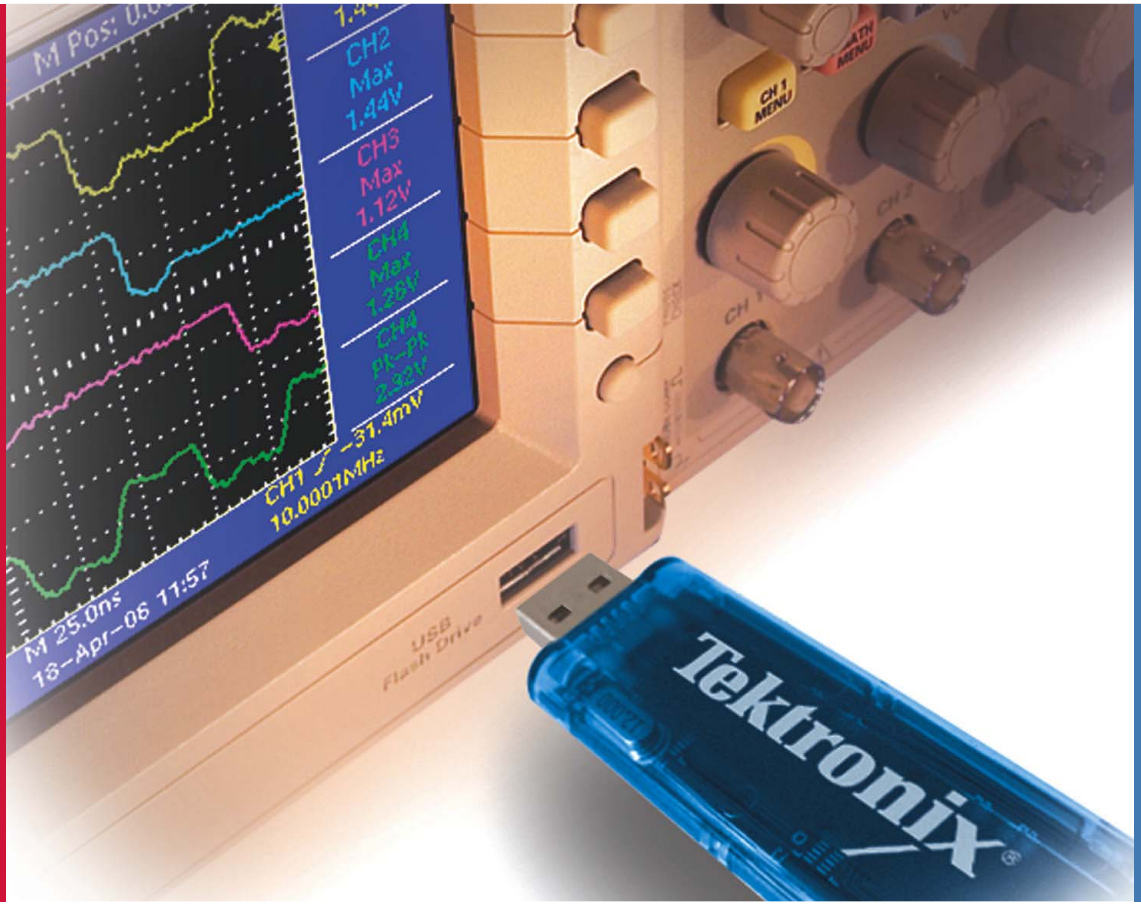

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Isolate your clock source

Isolating a clock between an oscillator and a load minimizes noise and other interference.

By Daniele Danieli, EUROCOM-PRO, Venice, Italy

Circuits such as PLL (phase-locked loop) synthesizers, high-dynamic-range ADCs (analog-to-digital converters), and timing-sensitive digital networks require a stable and spurious-free clock. Testing these circuits is often difficult if you use a master oscillator, even if the oscillator's signal meets the application's requirements for phase noise and spurious response. Variable clock-line loads and power-supply line interference—typical in the open-board environment on a lab bench—can degrade signal purity with jitter or unpredictable phase steps.

Insulating an oscillator from a load often requires a high reverse-attenuation buffer stage, which is difficult to implement at frequencies of 10 MHz and above. The circuit (**figure**) provides an isolated clock source using a high-speed optocoupler with low input-to-output capacitance. Isolating a clock source from its load eliminates ground loops that can introduce noise.

The circuit uses a quartz oscillator with two NPN transistors (Q1, Q2) that condition the oscillator's signal to TTL levels. The circuit also provides sufficient drive current for the optocoupler. The values of capacitors C3 and C4 are based on frequency. For example, at frequencies from 15 MHz to 30 MHz, you should use 220 pF for C3 and 100 pF for C4; scale up the values for lower frequencies.

The output of transistor Q3 will be a TTL-compatible signal. Select a value for resistor R7 to get the best pulse response. For most applications, you can use 22 Ω, but you can often omit R7 as well.

Having created a TTL-level signal, you can apply it to the input pin of IC2, which is a high-speed CMOS optocoupler such as the HCPL-7101, for frequencies up to 40 MHz. The HCPL-7101 provides an effective isolation from load conditions and electromagnetic interference.

The oscillator circuit and input side of the optocoupler use a dedicated battery to obtain the 5-V supply voltage. By using a battery, you won't add power-supply noise to the circuit. You can then connect the optocoupler's output side directly to your board under test—even with relatively long cables—without loading the oscillator stage. You can use any optocoupler of adequate bandwidth. Just make sure that your VCC voltage (regulator output) is compatible with the input-voltage specification for IC2. T&MW

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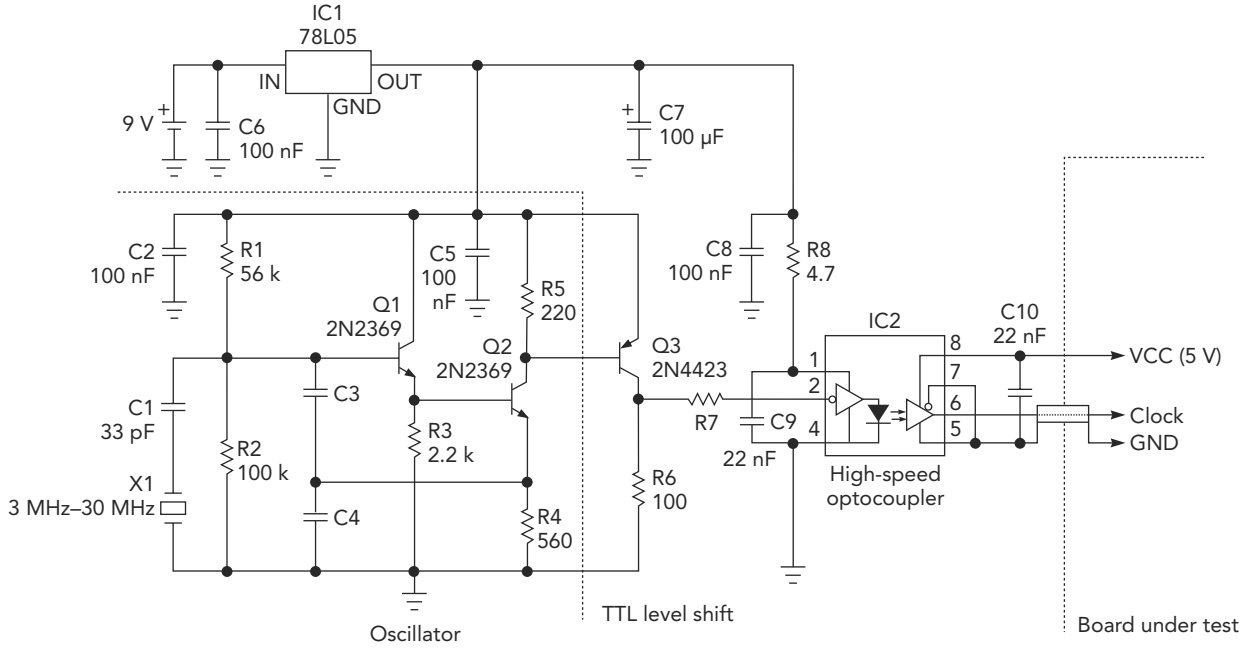


A high-speed optocoupler isolates a TTL-level clock source from ground loops and noise.

QUALITY by NEGOTIATION

ENGINEERS AT MERCURY COMPUTER SYSTEMS WORK TOGETHER TO FIND THE OPTIMAL BALANCE AMONG TEST, SIGNAL INTEGRITY, THERMAL ANALYSIS, MECHANICAL FIT, AND COMPONENT SELECTION.

BY MARTIN ROWE, SENIOR TECHNICAL EDITOR

CHELMSFORD, MA—For the past 25 years, engineers at Mercury Computer Systems have designed processor boards and systems for military applications, but yesterday's design and test methods no longer work. Higher functionality, increased heat, more sensitive signals, shorter design cycles, higher test coverage, and tighter budgets have all changed how the engineers perform their jobs.

To produce high-reliability products that must run for years in harsh environments, the various engineers at Mercury push for design details that often compete with each other. Test engineers, signal-integrity engineers, and mechanical engineers often negotiate with each other and with circuit and PCB (printed-circuit board) designers early in a design. The result: fewer board iterations, shorter design cycles, and more reliable products. By implementing new procedures, engineers have reduced the number of engineering change orders by a factor of 10.

In 2005, Mercury embarked on a DfR (design-for reliability) project for gathering input from all engineering departments and giving it to designers early in a design cycle. The program stemmed from the fact that many component suppliers were moving to lead-free processes, so Mercury needed to overhaul its entire design, analysis, and test practices. In addition, devices such as microprocessors and FPGAs (field-programmable gate arrays) were running faster while their size was shrinking, which increased heat density and threatened reliability.

Darryl McKenney, director of engineering services, was put in charge of the program. McKenney set out not only to give information to designers earlier, but also to automate the process. He started with component selection, the first part of the DfR project staircase that the company implemented. Since then, the company has implemented programs for all the functions and departments listed in **Figure 1.**

"The component turn from lead to lead free has been incredible," McKenney exclaimed. "It's the biggest change in electronics manufacturing since the move from through-hole to surface-mount components." At Mercury, the change to lead-free products affected more than 37,000 components that the company uses in its boards.

Evaluating new components

Because Mercury's boards are often used in military systems, which have long lives, many of the company's customers want designs that will remain unchanged for as

Test engineering supervisor Jim Ternullo and his team perform boundary-scan, flying probe, in-circuit, and functional tests on all new designs. They also provide feedback to circuit and PCB designers.

MARK WILSON

long as 20 years. The move to lead-free components, however, has made it impossible for Mercury to fulfill this request. The company must now develop new designs with new components.

When developing a design, Mercury engineers needed a method for calculating each component's effect on a PCB's reliability so they could eliminate any unacceptable lead-free parts from manufacturing. Gene Bridgers, principal reliability engineer, developed software that lets him calculate the MTBF (mean time between failures) of a board based on its components.

"We calculate MTBF using MIL-HDBK-217F1 and Telcordia SR332 standards," Bridgers said. "We make that data available to design engineers so they can calculate how a new component will affect MTBF. We advise designers about risky parts and provide ratings on those parts."

McKenney added, "If an engineer tries to select a component that lowers MTBF, we'll catch it. When we have a reliable part, we try to reuse it."

Mercury has also implemented a risk-rating system for components that all engineers can use to maximize MTBF. **Table 1** lists examples of low-, medium-, and high-risk parts. Components such as processors pose a high reliability risk because their designs are more likely to change than are the designs of resistors. When a semiconductor manufacturer announces a revision or discontinuation of a part, that decision can have a profound effect on Mercury's products.

For example, a processor or memory IC manufacturer may move to a smaller die size to reduce costs while at the same time making the part run faster. Both of those factors can increase the heat a device produces, making it less reliable unless the system provides additional cooling. A faster part can also result in timing errors.

Design changes that result from company buyouts can also affect a part's reliability. When a producer is bought by another company, the new owners may try to cut costs, often by moving manufacturing overseas. "Products made overseas may not be as reliable as those made in US," noted Bridgers.

(continued)

Get the heat out

Managing a board's thermal characteristics is perhaps the most challenging part of producing reliable PCBs. Finding the best placement for high-heat components such as processors and FPGAs is critical for keeping the devices cool.

As signal speed increases and die sizes shrink, ICs produce more heat per unit area (W/cm). "The thermal energy produced by a board has more than doubled in the last five years," said McKenney. He pointed out that the thermal specification for a PMC (PCI Mezzanine Card) that mounts on a processor board is 7.5 W. (PMC modules add processors or I/O to a mother board.) "We're designing PMCs that produce from 25 W to 30 W today." A full-height (6U) processor card produces 190 W of heat.

To combat the heat, mechanical engineering services manager Mike Gust and a team of mechanical engineers simulate the thermal characteristics of a board as soon as they know which components it will hold. They perform their analysis (**Figure 2**) while electronic designers develop schematics. Using Flotherm software from

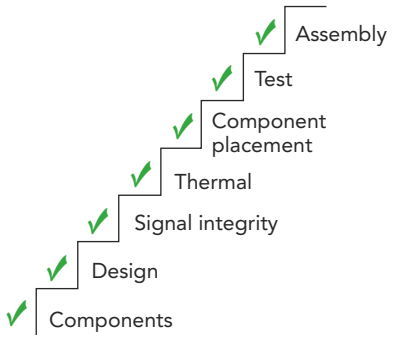


FIGURE 1. Mercury Computer Systems has implemented a design-for-reliability program in steps. Today, most of theses steps occur in parallel early in product design.

Flomerics, engineers including mechanical engineer Don Blanchet look for the best placement of components from a thermal perspective. In addition to performing heat simulations, Blanchet simulates air speed across a board. He can relay his findings to circuit designers and PCB designers before board layout begins.

To test the thermal simulations, Blanchet and others will create mockups of boards using the components slated for the final design. They can then measure temperature using thermocouples and Fluke dataloggers. They also use infrared cameras to create a heat profile of the board. "We place thermocouples on processors, FPGAs, and memory devices," said Gust. "Anything with a heat sink gets a measurement."

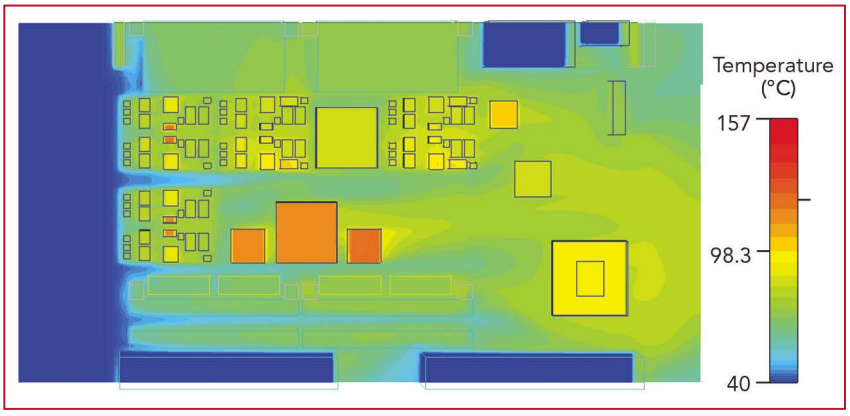


FIGURE 2. Simulation software lets engineers analyze a PCB for thermal characteristics and thus influence a PCB layout. Courtesy of Mercury Computer Systems.

When testing a design for thermal characteristics, Mercury engineers need powered devices. They also need software to exercise the parts. Software engineers create diagnostic routines that run the parts during a test. "Software routines should be a realistic representation of the worst-case heat that a device will likely produce in the field," commented Gust. "But there's no point in programming an FPGA to toggle all of its gates at once. That will never happen in the field."

Clean signals

Mercury's mechanical engineers can find the best component placement from a heat perspective, but they don't always get the placements they want. Signal integrity is also a factor in where a component will reside on a board. Signal-integrity engineer Paul Wade sees to that. Under the DfR program, Wade can influence where PCB designers place parts. Mercury's boards carry high-speed serial-bus signals such as RapidIO and PCIe (PCI Express).

Just as mechanical engineers simulate a board from a heat perspective, Wade simulates signals, looking for the best design. Using SIWave from Ansoft along with Spice simulations, Wade has automated the process. "Signal-integrity analysis used to occur when a board was 90% to 95% complete," he said. Now, Wade makes his case to the PCB designers at the start. He no longer spends most of this time fighting fires as he once did.

Because of the DfR program, tradeoffs between Wade and the thermal engineers happens early in a design. Wade tries to keep PCB traces as short as possible to minimize signal loss and jitter, but he often negotiates with the mechanical engineers. "People always ask if a signal trace can be 6-in. longer than I like," he said. "It's a constant tradeoff."

Wade has developed design rules to help PCB designers minimize signal-integrity problems. He has to explain that whenever data rates increase, the

Table 1. Risk classifications for typical components.

Risk classification	Types of components
Low	Capacitors
	Inductors
	LEDs
	Resistors
	Standard hardware
Medium	ADCs
	DRAMs and SRAMs
	Oscillators
	PLD ICs
	Standard cables
High	ASICs
	Fiber-optic transceivers
	Large memory devices
	Microprocessors
	Unique hardware

techniques that used to work will now cause problems. For example, he must tell PCB designers about the effects that vias through a board will have on signal integrity. At high frequencies, vias add to signal loss and add reflections to signals.

In 2009, Mercury's engineers will be using serial buses that run at 5 Gbps to 6 Gbps, about double the current speeds. That will have a profound effect on signal integrity and trace length.

As data rates increase, PCB materials absorb more energy. A PCB trace acts like a low-pass filter, limiting how much energy reaches a signal's destination. "We used to use PCB materials with loss-tangent specifications of 0.01 to 0.03," said McKenney. "Now, we need loss tangents of 0.008 to 0.009 because of the higher frequencies."

Like the mechanical engineers, Wade uses a mockup of a board design to verify his signal analysis. At the current data rates, he can analyze signals with a 6-GHz oscilloscope, but the higher data rates will require more bandwidth—at least 12 GHz. He also needs an oscilloscope with a 20-Gsamples/s acquisition rate to sufficiently capture the signals.

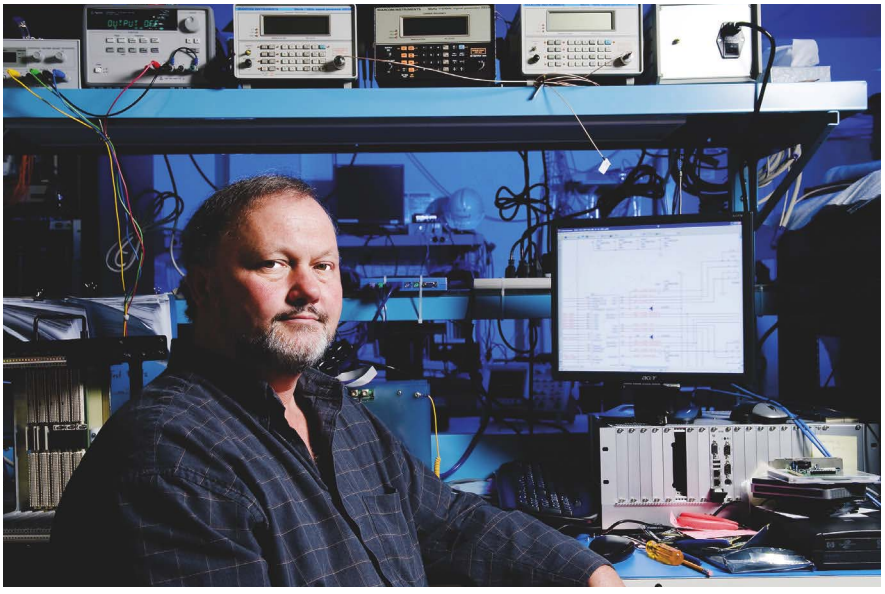
Wade uses a vector network analyzer to characterize signal traces on PCBs, measuring signal loss versus trace length. "The schematic doesn't tell the story," he said. "Schematics don't indicate trace lengths, nor do they show vias on a board." Both of these can cause voltage drops in high-speed signals. Furthermore, Wade noted that the spacing between traces has shrunk. At one time, all traces had 5-mil (0.005-in.) spacing, but that has dropped to 3.5 mil. The smaller spacing breeds more crosstalk between signals, which can increase bit errors.

His simulations also account for changes in temperature, not just because of device heating, but because some boards will operate in hot and cold environments. A signal's eye diagram will change depending on temperature. As temperature drops, signal edges get faster—overshoot and undershoot becomes more pronounced. Resistors increase their values with temperature, so Wade may need to ask for changes to the resistor values in a design.

Wade's work includes analyzing a board's power integrity. In the past, Mercury's boards used 12-V and 5-V power supplies, but today those boards have eight voltages ranging from 12V to 0.9V. At the low voltages, there's little margin for voltage dips without causing system failures. Thus, Wade must ensure that a board has enough properly placed bypass capacitors to minimize dips.

Having multiple switching power supplies and high-speed serial buses on a board opens the opportunity for switching signals to create bit errors. Wade must look at the interaction between power supplies and jitter that can cause bit errors.

The power supplies switch at around 600 kHz, yet they can cause errors on 3-Gbps serial data streams. To see those errors, Wade needs a deep-memory oscillo-



MARK WILSON

Manufacturing engineering manager Tom Orser uses optical and x-ray inspection to catch manufacturing defects before test engineers run board tests.

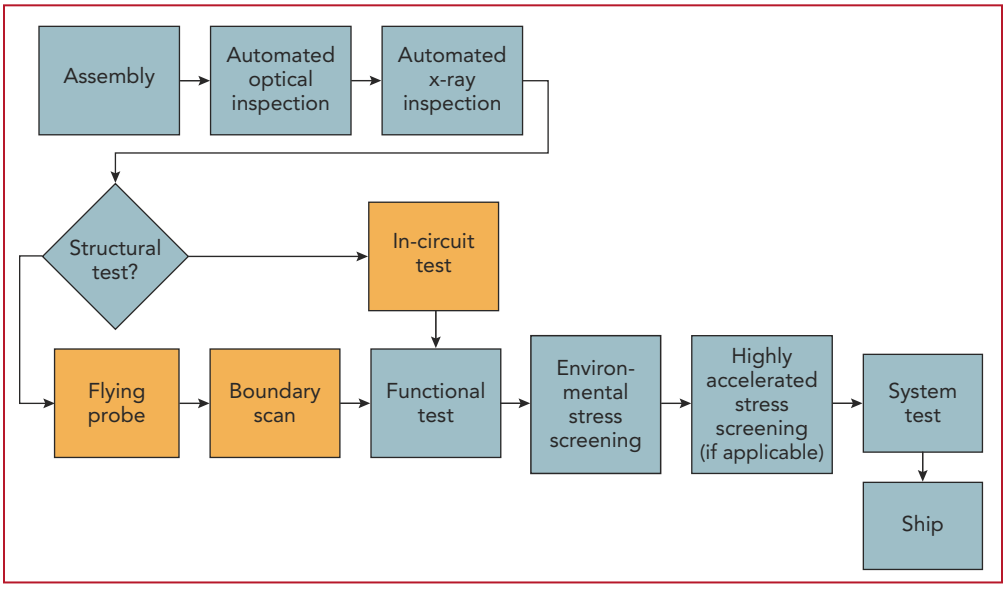


FIGURE 3. Test engineers have developed a test flow that produces structural test (orange boxes) and functional tests on processor boards.

scope to capture a few milliseconds of data at a 20-Gsamples/s rate.

McKenney said that design-automation tools such as those Mercury uses for thermal and signal simulation have improved dramatically over the last several years. Computer speed helps too. Simulations that used to take days now take hours. The simulations let engineers run "what if" scenarios before committing a board to a schematic.

Test's voice

At Mercury, test engineers also have a say in a PCB design because they need test points. Serial-port access to a board is also crucial for board configuration and diagnostics. Test engineering supervisor Jim Ternullo explained that test engineers work with circuit designers and PCB designers regarding the placement of test points. They review CAD files and schematics as well. They also work with diagnostic software engineers to get software to run functional tests. "We make sure that the PCB designers provide easy access to a board's serial ports," said Ternullo.

Mechanical engineering services manager Mike Gust and his team perform thermal simulations on boards and systems. They then measure temperature on processors, FPGAs, and memory devices.

MARK WILSON

Figure 3 shows the test flow that the engineers use when testing the Mercury boards. The boards first go through automated optical inspection and automated x-ray inspection, which, according to manufacturing engineering manager Tom Orser, catch most manufacturing errors before any tests.

Because of the company's low volume and high mix of boards, test engineers such as Roy Thompson use boundary scan to test as much of a board as possible. Thompson uses tools from Asset Intertech to develop and run boundary-scan tests. "All I need is a netlist from the PCB designer to start developing a boundary-scan test," he noted.

Thompson reuses test code wherever possible. The code starts as a software model of the board, which typically takes about two weeks to develop. But he noted that a model for DDR2 (double data rate) memory has taken as long as two months to develop, because the tests will operate the memory device outside of its operating specifications. Thompson

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runs boundary-scan tests at 8 MHz, far slower than normal operating speeds.

In places boundary scan won't cover, Mercury uses flying-probe testers and, in a few instances, in-circuit testers. The engineers use flying probes to test for shorts and opens. A flying-probe tester also measures component values such as capacitors and resistors with no power applied to the assembled board.

Although few boards get ICT (in-circuit test), Mercury engineers design them for that test anyway. "By the time we find out about a board's production volume, it's too late to design for in-circuit test so we have to design it in up front," said Ternullo. For boards that follow the ICT path, boundary-scan is performed as part of the test.

Flying-probe tests are easier to develop than in-circuit tests and they don't require an expensive test fixture, but they are much slower. A flying-probe test must check every node on a board, and a board can have as many as 2000 nodes. Each board can take as long as 45 min to test. But, as Ternullo pointed out, "Unless you have a $150,000 board and you build 20 or more a year, it doesn't pay to use in-circuit test." The cost of a test fixture often makes ICT cost prohibitive.

Either or both of these test methods are required because boundary scan can't test for everything on a board. Thompson said that 90% of Mercury's boards have at least 50% coverage with boundary scan. Under the DfR program, any new board with less than 90% coverage must get McKenney's approval to go into production.

Test engineers, signal-integrity engineers, mechanical engineers, and reliability engineers all have the means to influence circuit and PCB designers at Mercury Computer Systems. The company's DfR process provides a communication path and a system of checks and balances for making sure that each board is optimized for reliability, which encompasses thermal performance, signal integrity, and ease of test. T&MW

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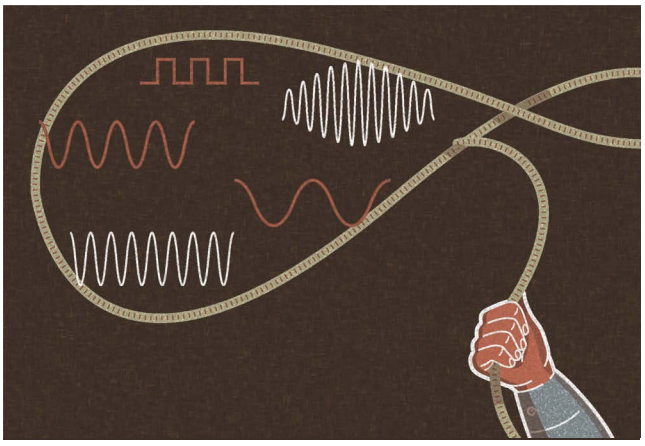

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TROUBLESHOOT intermittent signals

BY MIKE LAUTERBACH, LECROY

Engineers often spend considerable time locating and isolating intermittent signals. You may find that a design works most of the time, but an occasional unwanted condition causes the product to fail. You never want a case where you think you've solved a problem only to see it arise after many units ship to customers.

Most oscilloscopes have advanced tools that help you locate intermittent problems. You can use them when necessary, but you should start with the easiest method to track down a short pulse, slow rise time, or other unwanted signal characteristic.

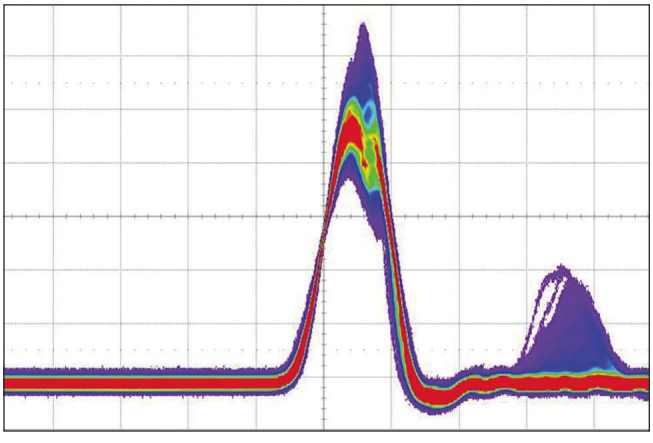

FIGURE 1. A color-graded persistence mode lets you see the frequency of a waveform's occurrence. A signal normally returns to its baseline after the pulse (red), but a secondary pulse occasionally occurs (blue and violet).

The value of persistence

The fastest and easiest way to spot a rare signal shape is through an oscilloscope's persistence mode. Many instruments use both intensity-gradient and color-gradient persistence. In intensity-gradient persistence mode, an oscilloscope will display a normal signal shape using bright pixels, and it will display rare (intermittent) occurrences with dim pixels. With color-gradient persistence, the most common signal shapes will appear in red. Less frequent events will appear in yellow and green, while rare events will appear in blue and violet. The waveform in **Figure 1** normally returns to its baseline following a pulse (red), but on rare occasions, an unwanted secondary, lower-amplitude pulse (blue and violet) occurs a short time later.

Once you find the abnormal signal shape, you should set up a trigger to capture it the next time it occurs. Triggers let you see the abnormal shape more clearly, and they let you check the operation of other devices at the same moment the failure occurs. If the failure occurs once per second, for example, then you should trigger the oscilloscope only when the failure occurs. You won't waste time looking at normal waveforms or clutter the screen with unnecessary information.

Use your knowledge of the intermittent signal shape to trigger when it occurs. Some of the most useful triggers for capturing intermittents are pulse width (sometimes called "glitch" to denote a very short pulse width), rise time (to spot edges that are too fast or too slow), runt (a piece of the signal with an amplitude that

is smaller than normal), and dropout (when a signal that should have steady activity stops having transitions).

Table 1. Statistics calculated for one slow signal reveal an abnormally short pulse width (shown in blue).

Measurement	Width	Rise time	Fall time
Value	165.180 µs	41.092 ns	38.327 ns
Mean	195.773 µs	42.441 ns	38.491 ns
Min	164.561 ns	39.292 ns	35.384 ns
Max	239.538 µs	118.305 ns	40.761 ns
Standard deviation	27.989 µs	3.2923 ns	854.04 ps

Move to the next step

Sometimes, an oscilloscope's persistence mode displays signal shapes all over the screen, but none that let you see the failure condition. If you can define the "normal" signal shape, then you may be able to set the oscilloscope to trigger only when a different condition occurs. You don't need to know the failure condition, just how to define a correctly shaped signal.

Suppose you are looking at a clock that shows excessive jitter at a certain frequency. You can tell the oscilloscope to trigger only when the time between two positive or two negative clock edges is outside a specified range. For example, a 100-MHz clock has a 10-ns interval, you might set the oscilloscope to trigger if a clock period is greater than 10.5 ns or less than 9.5 ns, but not trigger on clock signals in between those two values.

You can set up triggers based on pulse widths, intervals, duty cycles, rise times, fall times, and various other parameters, depending on your oscilloscope. **Figure 2** shows an example where the "staircase" in the waveform causes an unacceptable width between two rising or falling edges.

When you can't find an intermittent shape simply by viewing a waveform, you can get some clues about the error condition by using an oscilloscope's measurement statistics. With statistics, you don't need to know the failure condition of your circuit to make a guess at some parameters that could be affected by intermittent operation.

Suppose you've captured many triggered waveforms using a simple edge trigger and you use the oscilloscope to measure signal amplitude, rise time, fall time, pulse width, or other parameters. You can set the oscilloscope to display statistics denoting the maximum, minimum, and average values for each parameter. If you're hunting intermittent waveforms, you should look for minimum or maximum values that are unexpectedly far away from the average.

The **table** shows the statistics calculated by an oscilloscope on a fairly slow signal with a mean pulse width of 195.773 µs and rise times and fall times of around 40 ns. If you look at the data, you'll see a minimum pulse width of 164 ns—about *three orders of magnitude* shorter than normal. Because of that time difference, you won't see the short pulse while looking at the typical waveform characteristics—the pulse will be compressed due to the oscilloscope's time-base setting. Based on the statistics, you can set the oscilloscope to trigger on pulses of much shorter width (the time between a rising edge and the next falling edge) than normal and capture each occurrence of the error condition (**Figure 3**).

You can also use a histogram to get a clue about an error condition. Parameter statistics typically show the most recent value only, plus the average, minimum, maximum, and standard deviation. A his-

FIGURE 2. By setting a trigger that activates when a waveform characteristic is outside a range, you can ignore acceptable conditions and capture only error conditions, such as the "staircase."

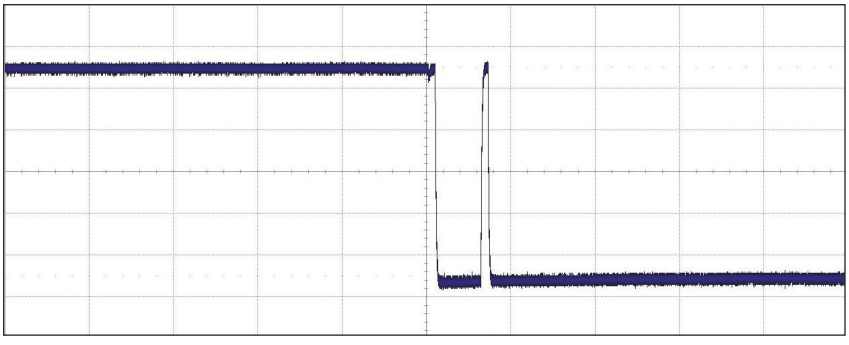

FIGURE 3. Triggering on pulse width lets you find narrow pulses, which you can then analyze by changing an oscilloscope's time-base setting.

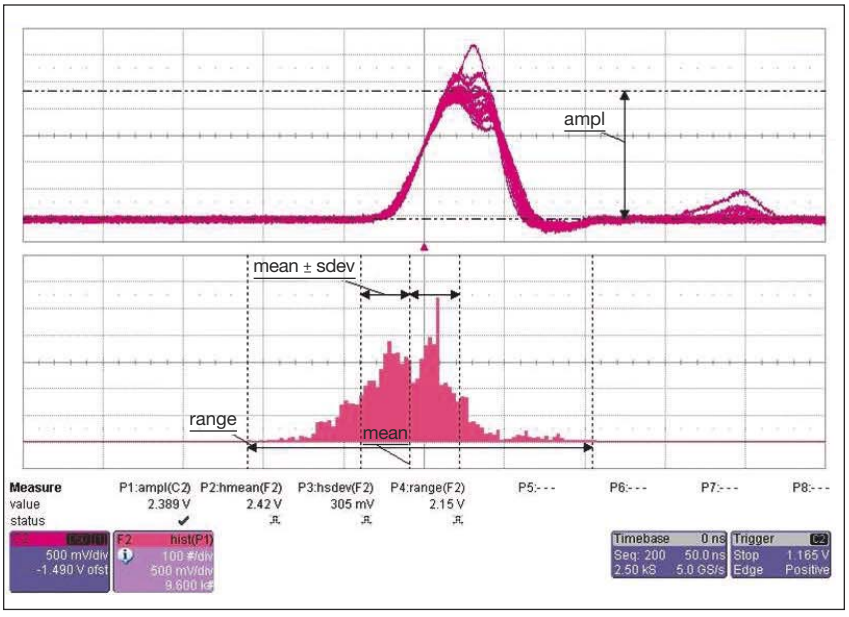

FIGURE 4. A histogram of parameter 1 (P1) shows the distribution of amplitudes. Rare events appear as long tails or small, separate peaks.

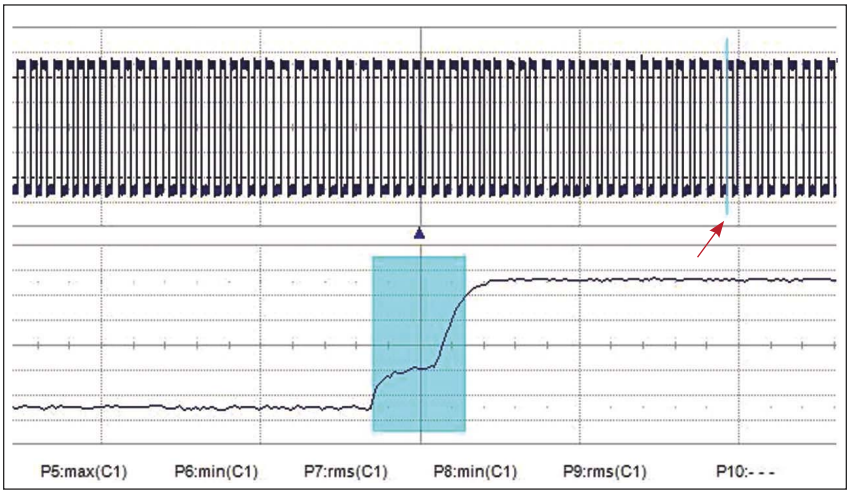

FIGURE 5. An oscilloscope can find an anomaly in a waveform's rise time (top, indicated by red arrow) and let you zoom in on it (bottom).

togram will display all the measured values of the parameter. Histograms let you count the rate of bad events, and you can put a cursor on the histogram to read the value of the offending signal shape. Thus, you can set up a trigger for that type of event.

Figure 4 shows an aberrant signal that appears in the tails of a histogram of a signal's amplitude. The long tails indicate that occasionally one amplitude is considerably higher or lower than most others.

Sometimes, you need an oscilloscope to find an extremely rare shape in a captured waveform. Consider the upper trace in **Figure 5,** where a particular rise time occurs just once on the captured waveform. You can set the oscilloscope to search for signal characteristics that fall inside or outside a certain range. The undesired edge on the signal in the figure may occur because the signal got caught between pull-up and pull-down states, causing the edge to pause in its upward deflection.

You can also use an oscilloscope to monitor a live signal, scan the signal for unusual signal shapes, and stop on an occurrence and save the screen image. Just set the oscilloscope to the sort of signal characteristic you would like to capture. The oscilloscope will monitor the live

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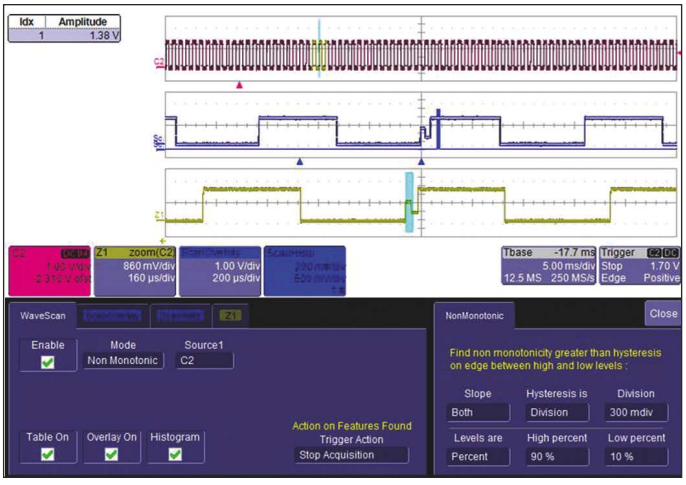

FIGURE 6. Oscilloscopes let you monitor live waveforms (top trace) and zoom in on an intermittent failure such as a short glitch in the middle of the rising edge (bottom trace). The middle trace shows an overlay of several acquisitions in which a non-monotonic edge was found.

signal until it finds an occurrence. The oscilloscope can then stop with this waveform on the screen or archive it for later viewing and analysis and continue to look for more occurrences.

Figure 6 shows an example where the oscilloscope watches live data for non-monotonic edges (in either direction). When one occurs, the oscilloscope captures the waveform in the top trace, and a zoom shows the details in the bottom trace.

Intermittent signal failures have long been a nemesis for design and test engineers. Today's digital oscilloscopes offer a variety of tools that help engineers locate and troubleshoot the sources of these problems. Some of the tools are quite simple, requiring only a single button push. When the simple methods fail, you can use more advanced tools. Yet, even the advanced tools are fairly simple to set up and often give more insight into circuit behavior. T&MW

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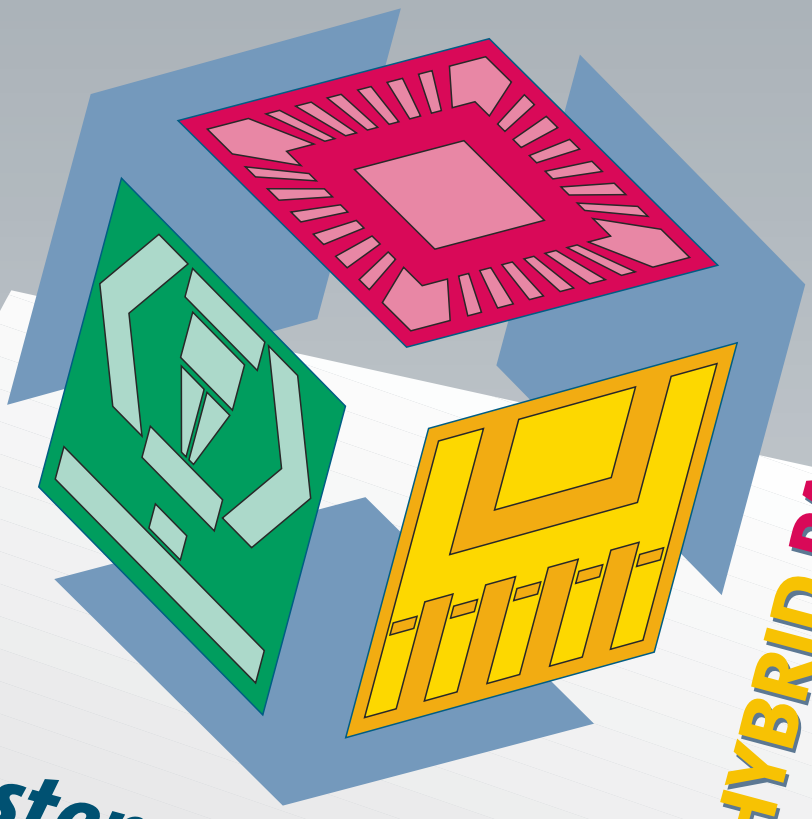

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DIGITAL SIGNAL COMPRESSION IN MIXED-SIGNAL ATE

Compression techniques can reduce real-time waveform memory requirements or increase the performance of test instruments.

DANIEL ROSENTHAL, 3 DB CONSULTING

Signal compression is an appealing technique to use in mixed-signal ATE (automated test equipment) systems because it can reduce the cost of test while improving tester performance. Unfortunately, mixed-signal ATE is one of the last remaining class of systems where designers still cling to the comfort of uncompressed, fixed-rate linear coding.

It was fairly common for manufacturers to compress the signals on older analog testers and then accept and manage the resulting error budgets and uncertainty. But once AWGs (arbitrary waveform generators), digitizers, and DSPs (digital signal processors) were combined to create mixed-signal testers, many in the industry began treating digital-domain signals with absolute exactness.

In contrast, manufacturers of other types of DSP-based systems have embraced more efficient coding techniques: Telecom systems have long used voice-band coding (ADPCM, or adaptive differential pulse code modulation); imaging systems are coded with JPEG; video employs MPEG; and audio systems, of course, use the ubiquitous .MP3 format. The use of these compressed coding techniques has made the economics of digital media distribution practical.

The benefits of signal compression to mixed-signal ATE are many. Most obviously, signal compression allows manufacturers to build a system with less storage memory, leading to lower system cost. Conversely, this advantage could be turned around to yield greater waveform capacity. Compression can reduce the required number and quality of signal interconnects, which consume a significant portion of ATE system real-estate and material costs. In addition, a 4:1 compression can also increase the effective performance of existing interconnects by allowing a 5-GHz infrastructure to support 20-GHz instrumentation.

Bandwidth and Nyquist

ATE system bandwidth is dictated by the Nyquist theorem regarding analog signals (bandwidth < Fs/2, where Fs is the sampling frequency) and the quantization-noise-limited SNR (signal-to-noise ratio). For example, SNR in dBfs (decibels full scale) = 6.02 ENOB + 1.76, where ENOB is the effective number of bits. Both anti-

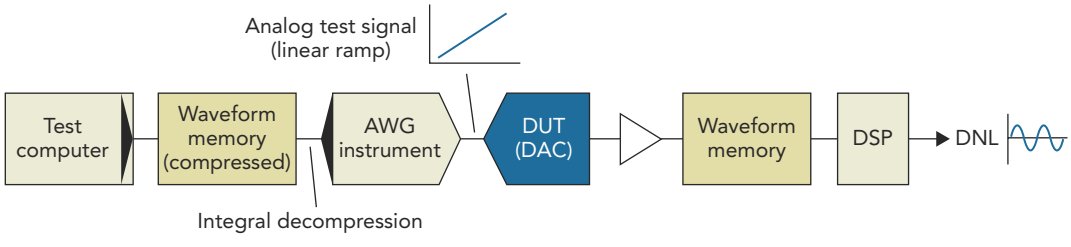

FIGURE 1. Lossless compression cuts memory requirements in a DAC linearity test without compromising accuracy or increasing uncertainty.

aliasing and reconstruction filters, however, require higher oversampling rates to be used, further driving up memory size and interconnect bandwidth.

Some systems use encoding techniques such as block floating point or DSP techniques such as decimation, but these cannot approach the ideal sample rates dictated by Nyquist.

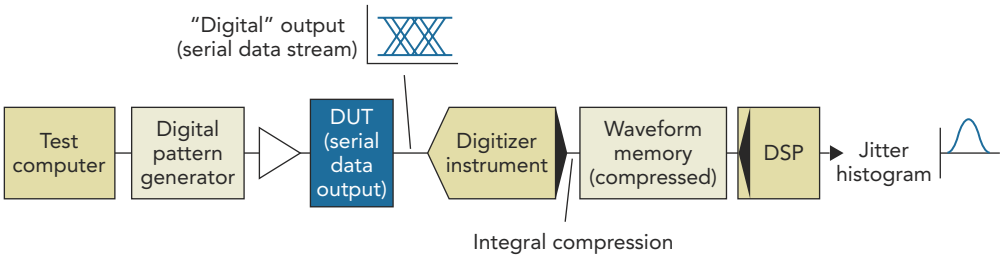

FIGURE 2. For a serial-data test signal, the application of 8:1 lossy compression resulted in a change in the jitter error measurement of less than 3%.

Designers of mixed-signal ATE systems generally still prefer uncompressed, fixed-rate linear coding. The engineers who resist using signal compression are often concerned about three main issues: measurement accuracy and uncertainty, a compression method's ability to handle arbitrary (and unknown) measurements, and the ease of integrating the compression algorithm into a system. But these concerns are easily addressed by capabilities in today's commercial signal-compression algorithms, so designers should not hesitate to incorporate compression into their mixed-signal testers.

For example, at the most basic level, some compression algorithms perform lossless compression, which permits the original signal to be recovered from the compressed signal. While the use of lossless compression will not affect measurement accuracy and uncertainty, the resulting compression ratio could greatly reduce the system cost and footprint. An example of a mixed-signal test in which lossless compression can achieve this objective is an all-codes DAC (digital-to-analog converter) linearity test, in which thousands of samples are reduced to one or two numbers representing the worst-case integral or differential linearity of the device under test. The integrity of the measurement depends on accurately preserving the tested parameter, not on accurately preserving every single analog sample.

Tests of compression algorithms

While working with Samplify Systems, I helped the company conduct tests of its commercially available signal-compression algorithm. One DAC linearity test (**Figure 1**) that used the algorithm achieved a 5:1 lossless compression ratio of the simulated data with no loss of accuracy or uncertainty. We included noise at the –90-dBfs level and 0.1% nonlinearity in the evaluation signal to approximate actual device errors and ATE system noise.

As is the case with other compression technologies, using lossy compression, in which the original signal is "lost" and cannot be fully recovered, can yield significant increases in the compression ratio, while the losses remain imperceptible to the user. In another test of the Samplify algorithm, in which we measured jitter on a simulated high-speed serial data signal, we used a test signal that was a noisy square wave with added jitter (σ = 1 sample). We analyzed the data by estimating the probability distribution function of the zero crossing with respect to time and then deriving the probability density function. We then measured the standard deviation, providing an estimate of the RMS (root mean square) jitter (**Figure 2**).

In this example, 8:1 lossy compression resulted in a change in the jitter error measurement of less than 3%. Note that, once quantified, uncertainty introduced by a data-compression process can be managed at the system level just like any other error term. In these cases, the errors are certainly acceptable.

These two examples involved specific types of mixed-signal measurements where compression achieved compelling results. Some engineers, though, are concerned about whether compression can achieve meaningful results when the signals are unknown or arbitrary. After all, the original motivation for basing mixed-signal ATE instrumentation on AWGs and digitizers was to have a tester that engineers could adapt to new tests by simply changing the DSP algorithms rather than by installing new test hardware. Again, due to the practicalities of reconstruction and anti-aliasing filters, these reconfigurable systems must operate in an oversampled mode, and test-program designers

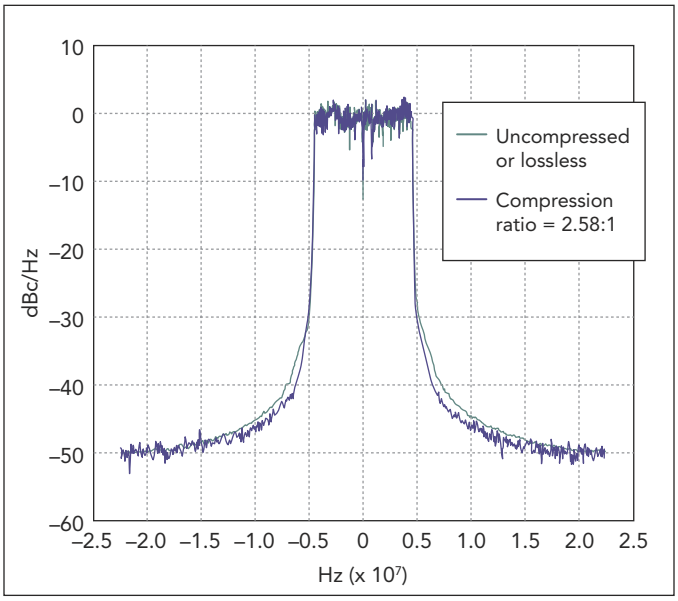

FIGURE 3. While the compression ratio may vary depending on the test signals to be generated or measured, compression applied to this simulated OFDM waveform, for example, can offer bit-rate reductions that achieve or better that of ideal Nyquist sampling.

must still develop customized resampling DSP algorithms for the signals under test. To achieve sample rates close to the Nyquist rate, these resampling algorithms become extremely complex.

Because compression is transparent to the signals under test, once compression resides in the digitizer, and decompression in the AWG, you no longer need customized DSP algorithms for each test and signal set. While the compression ratio may vary depending on the test signals to be generated or measured, compression can offer bit-rate reductions that achieve or better the bit rates of ideal Nyquist sampling.

For example, **Figure 3** illustrates a simulated OFDM (orthogonal frequency-division multiplexing) waveform for testing a WiMAX baseband SOC (system-on-chip) device. Typically, the ADCs (analog-to-digital converters) operate at 2X oversampling of the signal centered at Fs/4. Lossless compression achieved a compression ratio of 2:1, which is equivalent to the ideal Nyquist sampling rate. Because the ADCs on the SOC may have only nine effective bits of resolution, however, you can achieve a compression ratio of 3:1 by operating the compression algorithm in a fixed quality mode to maintain 54 dB of SNR.

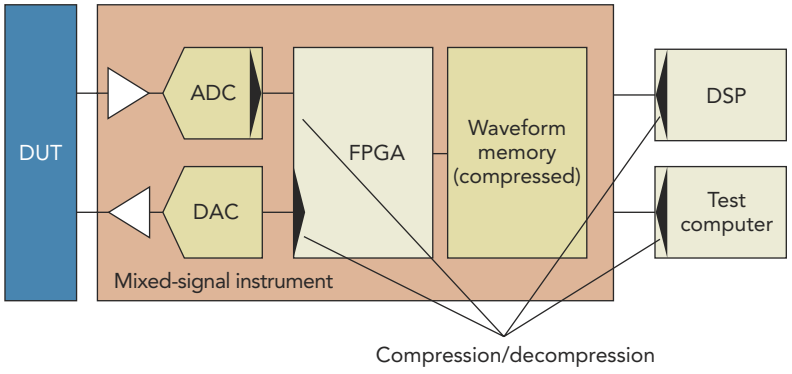

FIGURE 4. Nearly all digital signal I/O from ADCs and DACs in mixed-signal ATE connects to FPGAs, providing a convenient and straightforward place to introduce signal compression.

Unlike traditional sampling techniques, compression achieves these bit-rate reductions while maintaining the original timing resolution. Hence, compression extends the capabilities of general-purpose testers based on AWGs and digitizers without requiring designers to develop customized DSP algorithms for each test. *(continued)*

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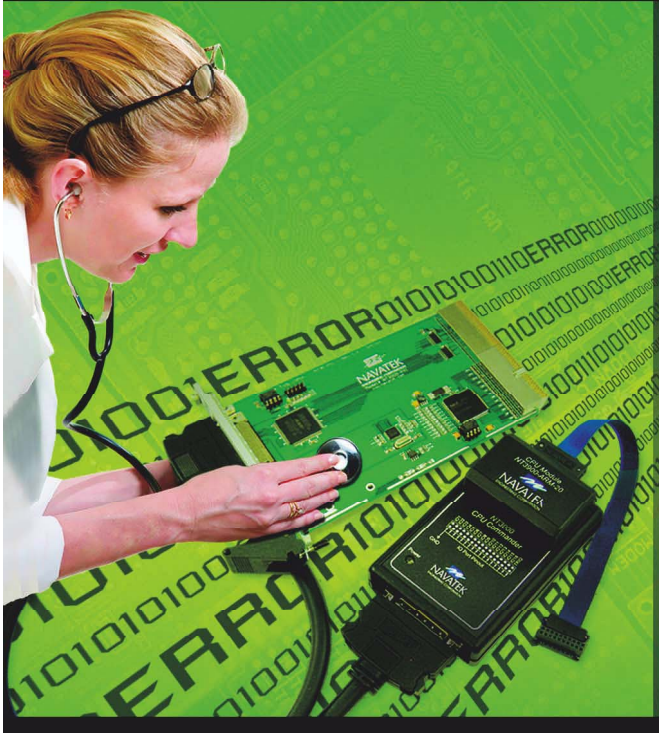

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To simplify the integration of high-speed signal compression into mixed-signal ATE systems, commercial algorithms are available in several forms. Examples include:

- software libraries for general-purpose computers,
- modules for computing software packages,
- FPGA (field-programmable gate array) cores, and
- data converters with integrated compression.

Signal-compression algorithms implemented as FPGA IP (intellectual property) or embedded in a data converter are particularly appropriate for mixed-signal ATE, because many ATE systems already use FPGAs and data converters. In fact, nearly all digital signal I/O from ADCs and DACs in ATE equipment connects to FPGAs, making either a converter or the FPGA a convenient place to introduce signal compression (**Figure 4**).

By taking advantage of compression algorithms to incorporate signal compression into a mixed-signal ATE system design, manufacturers will realize savings in the cost of data storage and interconnect complexity as well as in the cost of test program development. Designers need no longer fear that compression will negatively affect measurement accuracy and uncertainty. T&MW

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Daniel Rosenthal *founded 3 dB Consulting in 2005; the firm provides design services to providers and users of analog and mixed-signal instrumentation and has provided consulting services to Samplify Systems. Prior to that, he held various senior technical and managerial positions at Teradyne, Schlumberger, Applied Materials, and FEI. Rosenthal is named on five patents related to mixed-signal instrumentation and holds a BSEE from Cornell University. drosenthal@3dbconsulting.com*

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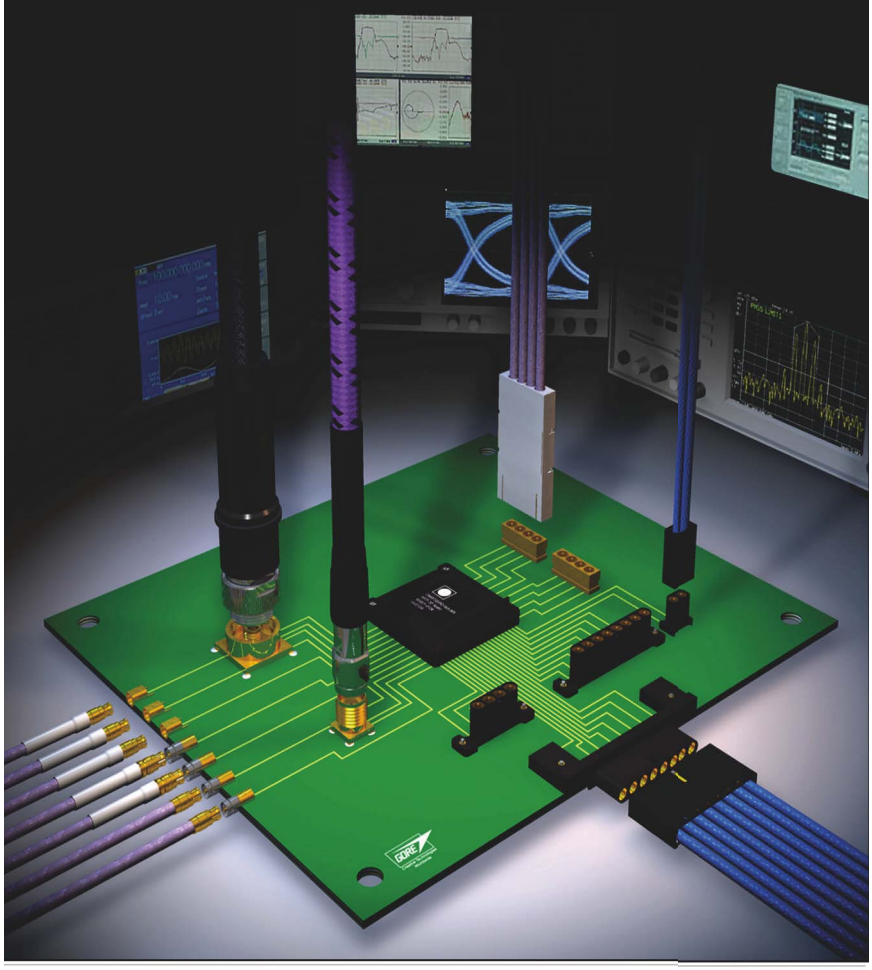

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Peak power meters offer high sampling rate

By combining a 20-MHz bandwidth with a 64-Msamples/s sampling rate, Anritsu's new ML2480B series peak power meters can conduct peak-power measurements on wireless and military-communications signals. The new meters target the evaluation of chipsets, modules, handsets, CPE (customer premises equipment), and base stations during R&D and manufacturing.

The two meters in the series are designed to measure average power, peak power, and crest factor, as well as provide statistical analysis of complex modulated signals. The ML2487B supports a single sensor input while the ML2488B supports dual sensor inputs. The dual-channel sensor input and display of the ML2488B allow for the simultaneous monitoring of WLAN and Bluetooth-enabled devices.

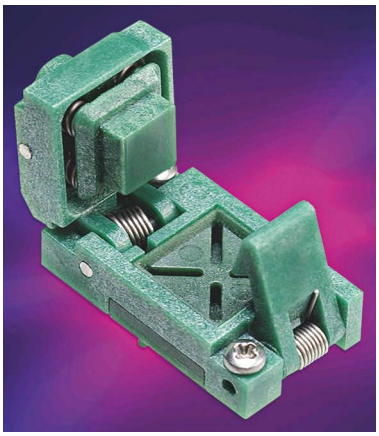
The ML2480B series instruments include an Ethernet remote-control interface and an external video port that supports LCD and CRT monitors. A remote GUI called PowerMax provides an enhanced instrument display and streamlines remote control. PowerMax allows measurement results for up to eight gates and up to four marker readings to be simultaneously displayed on a monitor. The software also creates configuration tabs so the instruments can be easily controlled directly from a PC. Measurement result images and traces can be saved directly on a computer's hard drive or removable storage, allowing raw data to be recalled and used as a reference.

Six families of continuous wave, average, wideband, pulse, and thermal power sensors that operate to 50 GHz are compatible with the ML2480B series.

Base prices: ML2487B—$5270; ML2488B—$6220. *Anritsu, www.us.anritsu.com.*

Aries debuts 6.5-mm center probe test socket for test and burn-in

Aries Electronics has introduced a high-frequency center probe test socket in a standard molded format that enables the socket to accommodate any 6.5-mm or smaller CSP, MicroBGA, DSP, LGA, SRAM, DRAM, or flash device.The socket is available with machined or custom-molded pressure pads and interposers, and its pressure pad compression spring allows for height variation in device thickness and provides proper force against the device. The socket can be easily mounted to and be removed from a PCB (printed circuit board) using two stainless-steel mounting screws.



The spring probes feature contact forces of 15 g per contact on 0.30-mm to 0.35-mm pitches, 16 g per contact on 0.40-mm to 0.45-mm pitches, and 25 g per contact on 0.50-mm pitches or larger. The socket offers less than 40 mΩ of contact resistance, an operating temperature range of –55°C to 150°C, and a contact life of an estimated 500,000 cycles minimum.

Base price: 100-lead socket—$125. *Aries Electronics, www.arieselec.com.*

Thermometer handles different probes

The Models 1523 and 1524 reference thermometers from Fluke/Hart Scientific bring laboratory quality measurements to the field through PRT (platinum resistance thermometer), thermocouple, and thermistor probes. The single-channel 1523 and dual-channel 1524 feature an accuracy of ±0.002%, and they will hold that accuracy over an ambient temperature range of –10°C to 60°C, with the dual-channel model 1524 able to measure the temperature difference between its probes.

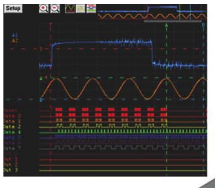
The thermometers can log data, storing up to 15,000 time-stamped measurements that you can download to a computer. The meters also plot data and perform statistical analysis on temperature data.

Prices: Model 1523—$1425; Model 1524—$1700. *Fluke, www.fluke.com.*

Turn your PC into an MSO

The MSO-9212 mixed-signal oscilloscope connects to a PC through its USB port and provides two analog and 12 logic channels. The instrument samples at 1 Gsample/s when running one analog channel and at 500 Msamples/s when using both. It maintains the 500-Msamples/s rate when using both analog channels and all 12 logic channels, with 200 Msamples of acquisition memory available for each channel with all 14 channels operating. The logic channels are disabled when the instrument runs a single analog channel at 1 Gsample/s. The instrument has an analog bandwidth of 200 MHz.

Using the PC software, you can set the MSO-9212 to trigger on analog channels, digital channels, or a combination of both. Triggers include level, edge, glitch, pulse width, and count. Digital triggers include logic levels and edges as well as triggers for the SPI (serial peripheral interface) I²C serial buses. The MSO-9212 will also decode data on these serial buses.



The software also lets you run FFTs (fast Fourier transforms) on analog signals, converting them to the frequency domain. Then, you can save the frequency-domain data for further analysis. The instrument can make up to 40 kinds of waveform measurements including frequency, peak-to-peak, duty cycle, rise time, and fall time. A channel-history feature lets you display the 30 most recent signal acquisitions. Color codes indicate relative time of acquisitions.

Price: $1799 (includes two 300-MHz passive probes, a USB cable, and an AC adapter). *Link Instruments, www.linkinstruments.com.*

Universal T1/E1 card

GL Communications has added a universal T1/E1 PCI 2.1-compliant card to its T1/E1 analyzer hardware and software test suite with Release 5.13. The universal board can process hundreds of channels or time slots simultaneously on T1 and E1 lines.

Unlike previous versions, which required separate boards for T1 and E1, the new card has integrated hardware support for both types of lines, allowing easy switching between T1 and E1 interfaces. What's more, it can be plugged into either a 5-V or 3.3-V PCI bus slot. The new board is also smaller than its predecessors, with dimensions of just 4.2x7.1 in. The use of direct memory access and a 32-bit–wide bus make it faster and more efficient than the older boards.

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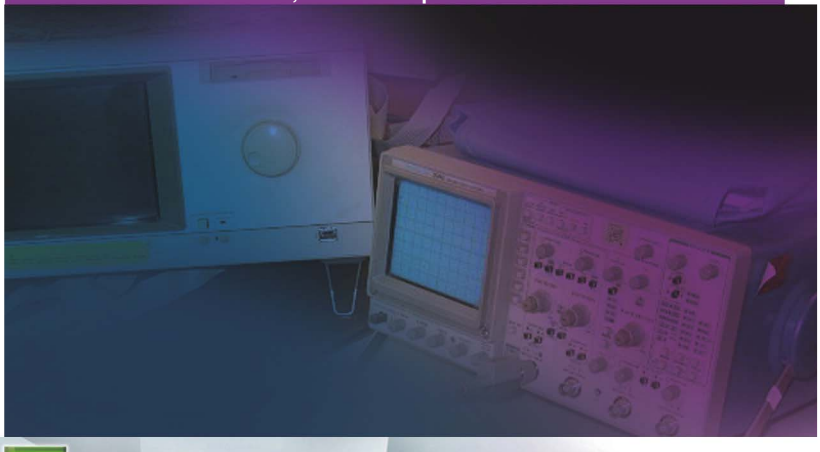

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Miro 4

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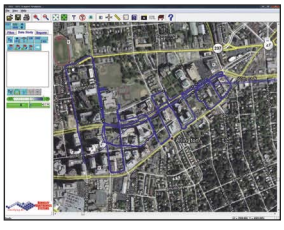
The universal card features in-service monitoring and emulation of T1 and E1 circuit connections. It provides out-of-service troubleshooting, such as bit-error-rate testing, alarm monitoring, signaling bit manipulation, DTMF/MF generation and detection, and drop and insert capabilities.

GL Communications, www.gl.com.

Software performs WiMAX site surveys

Running on the YellowFin WiMAX analyzer, DragNet mapping coverage software from Berkeley Varitronics Systems lets you perform drive studies and post-processing analysis of your WiMAX networks while still in the field. The program combines real-time YellowFin WiMAX measurements with GPS geo-coding accuracy.

You can create survey bitmaps with Berkeley's GPS Projector software. Next, drive to any spot with GPS reception, while DragNet Collector scans selected Mobile WiMAX channels and correlates them to your exact location automatically via GPS. The GPS measurements provide both latitude and longitude, as well as time stamps, for a complete WiMAX survey path anywhere in the world. Survey data, such as RSSI, cell ID, and segment ID, can be exported into DragNet's Analyzer for further mapping coverage studies in multiple graphical and tabular layouts. In addition, you can export surveys into KML (Keyhole Markup Language) files for plotting in applications like Google Earth.



Berkeley Varitronics Systems, www.bvsystems.com.

Expanded dual-channel DSO line

Two new models join B&K Precision's line of dual-channel DSOs (digital storage oscilloscopes): the 60-MHz Model 2540 and the 100-MHz Model 2542. The company says that with their low price tags ($940 for the Model 2540 and $1155 for the Model 2542), the instruments are among the most aggressively priced scopes on the market. The compact oscilloscopes offer a color LCD, front-panel USB port, analog-style knobs and controls, and one-touch automatic setup.

B&K Precision, www.bkprecision.com.

Entry-level fiber-optic test tools

JDSU's c-Series of compact photonic test tools for the development and manufacture of fiber-optic connectors and passive components provides an entry-level alternative for engineers who require simple, single-function testers. The c-Series includes the

cOPM-A1 optical power meter, the cFPL-A1 Fabry-Perot light source, and the cORL-A1 optical return loss meter.

The general-purpose bench testers are entry-level instruments designed for new labs and for engineers just entering the industry, as well as for small- and medium-sized manufacturers of connectors and patchcords.

JDSU, www.jdsu.com.

OEM version of USB module

The DT9812 family of USB data-acquisition modules from Data Translation now includes an OEM version that allows users to embed the board into their own systems. The DT9812-10V-OEM board, which has no enclosure, provides two 20-pin connectors to accommodate all I/O signals.

Like the enclosed models in the DT9812 family, the DT9812-10V-OEM furnishes eight analog inputs, two analog outputs, 16 digital I/O lines, and one 32-bit counter/timer. Both the analog input and analog output subsystems have 12-bit resolution and throughput rates of up to 50 ksamples/s. The board also provides an analog input and output signal range of ±10 V and can generate sine, rectangle, triangle, or DC waveforms with the analog outputs. Power is derived from the USB, so no external power supply is needed.

Price: $349. *Data Translation, www.datatranslation.com.*

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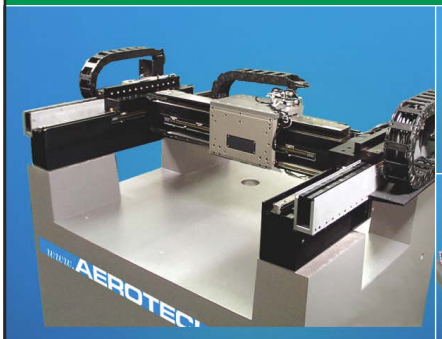

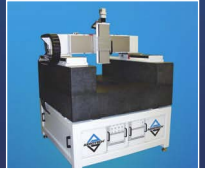

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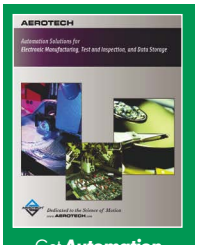

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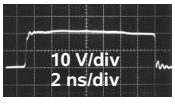

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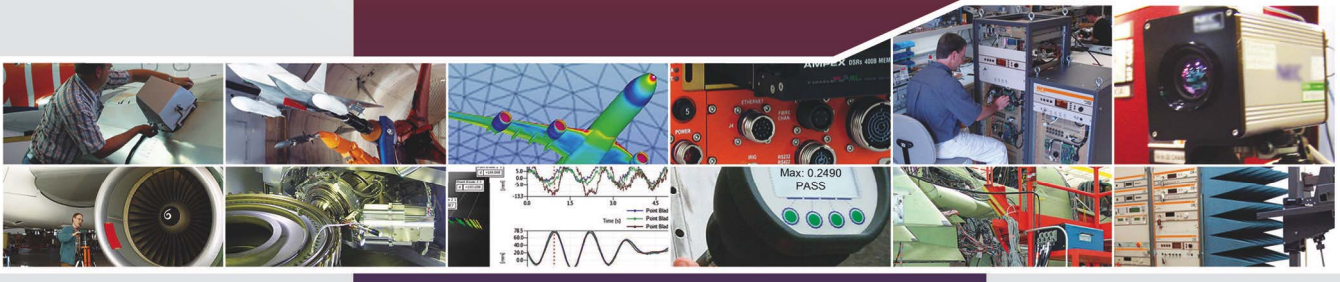

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CATALOGS & PRODUCTS

The following write-ups were supplied by advertisers in this issue.

Dynamic signal analyzer

The CoCo-80 handheld dynamic signal analyzer has two to 16 input channels with a 130-dB dynamic range. It can continuously record the time signals while performing spectral analysis, octave analysis, or order tracking. *Crystal Instruments, www.go-ci.com.*

Fast pulse tests

Avtech's new "Web Guide & Short Form Catalog 17S" outlines the company's family of high-speed (40-ps to 100-ns rise time), high-current (0.1 to 500 A), and high-voltage (2 to 3000 V) pulse generators, drivers, and amplifiers for research and production testing applications. *Avtech Electrosystems, www.avtechpulse.com/literature/cat17s.pdf.*

Gore configuration tools

Gore's interactive, online design guides provide step-by-step instructions for configuring RF/microwave assemblies, Gore High-Flex round or flat cables, Gore Trackless cables, and Gore UHD interconnects. *W.L. Gore & Associates, www.gore.com/designcenter.*

Accurate temperature measurement

TEMPpoint is a temperature-measurement instrument designed for high accuracy and industrial robustness. The instrument allows direct thermocouple, RTD, and precision voltage measurements with a PC. USB and Ethernet (LXI) versions are available. *Data Translation, www.datx.com/products/instruments/temppoint/default.asp.*

Multiport S-parameter ATE

In-Phase has developed a tester that performs fully error-corrected S-parameter characterization at the DUT input plane. Software and hardware connect any DUT port to port 1 or port 2 of a vector network analyzer. Software allows users to configure tests to report averages and totals. *In-Phase Technologies, www.in-phasetech.com.*

Conducted immunity system

The Model CI00250 contains all the equipment needed to perform conducted immunity testing to the IEC 61000-4-6 specification. This self-contained system includes a signal generator, a two-channel power meter, a 75-W amplifier (10 kHz to 250 MHz), and control software. *AR RF/Microwave Instrumentation, www.ar-worldwide.com.*

Versatile bench multimeters

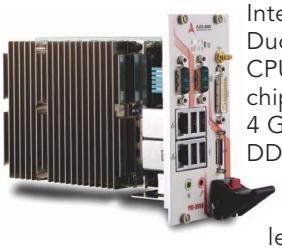
The 8845A/8846A 6.5-digit meters are ideal for R&D or automated test systems. The 8808A 5.5-digit meter is designed for manufacturing, development, and service. *Fluke, www.fluke.com.*

Test/burn-in & RF sockets

New CSP/BGA test/burn-in and RF sockets from Aries Electronics accommodate pitches down to 0.3 mm for use with an even greater range of CSP, MicroBGA, DSP, LGA, SRAM, DRAM, and flash devices. *Aries Electronics, www.arieselec.com.*

Dual-core PXI controller

Adlink has announced the PXI-3950, a dual-core PXI controller with an Intel Core 2 Duo T7500 CPU GME965 chipset and 4 Gbytes of DDR2 memory for the highest level of performance. *Adlink Technology, www.adlinktech.com.*



DC power apps poster

A poster from Agilent Technologies describes DC power-analysis applications and solutions across various industries. To celebrate the seven industry awards it has earned, Agilent is offering a 14% discount for a limited time. *Agilent Technologies, www.agilent.com/find/N6705A_Promotion.*

USB serial adapters

Sealevel Systems is offering one- and two-port USB serial adapters that are software-configurable for RS-232, RS-422, or RS-485. The adapters eliminate the need to open the enclosure to change jumper settings or dip switches. *Sealevel Systems, www.sealevel.com*

Design a switching system

Dow-Key Microwave has released three application notes that describe how to build a switching system with the company's CANbus switches together with an Ethernet or a GPIB kit. The AN2008-08-CYOM note describes the hardware, while AN2008-08-ENET and AN2008-08-GPIB explain the software control. *Dow-Key Microwave, www.dowkey.com/publications.php.*

Low-frequency VNA

The wide frequency range (1 Hz to 40 MHz) of the PC-controlled Bode 100 vector network analyzer is ideal for many RF and low-frequency applications such as control circuit analysis. *Omicron, www.omicron-lab.com.*

New DAQ brochure

Measurement Computing's new product flyer presents the company's latest PC-based data-acquisition and control hardware and software. The publication features nine new USB and two PCI Express products. *Measurement Computing, www.mccdaq.com.*

Pressure-compensation device

With its NEMA 3 rating, the DA084 pressure-compensation plug is ideal for automotive applications, where it permits a controlled change in pressure in enclosures that house electronic components. The plug protects against pressure differentials that can cause an enclosure to absorb dust. *Omega Engineering, www.omega.com.*

Three-state attenuated switch

Ideal for test and measurement, the CAS-37 attenuated switch eliminates the need for external cables or attenuators. The CAS-37 provides three states: through path (low loss), attenuated path (known high loss), and open state (with path for user to ground). *Teledyne Relays, www.teledynecoax.com/pressreleases/3-state.asp.*

Vector signal analysis

Tektronix says you can get the functionality of a vector signal analyzer and a spectrum analyzer as well as the powerful trigger capabilities of a digital oscilloscope in a single package with its SignalVu vector signal analysis software. *Tektronix, www.tektronix.com/signalvu.*

Mobile lab furniture

From large freestanding benches to height-adjustable tables and compact equipment carts, Anthro manufactures lab furniture that is strong, mobile, easy to configure, and supported by a lifetime warranty. *Anthro, www.anthro.com*

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15. Extent and Nature of Circulation:	Average No. Copies Each Issue During Preceding 12 Months	No. Copies of Single Issue Published Nearest Filing Date
a. Total Number Copies *(Net Press Run)*	55,857	55,728
b. Legitimate Paid and/or Requested Distribution (by Mail or Outside the Mail)		
1. Outside County Paid/Requested Mail Subscriptions stated on PS Form 3541.	52,485	51,809
2. In-County paid/requested mail subscriptions stated on PS Form 3541.	0	0
3. Sales Through Dealers and Carriers, Street vendors, Counter Sales and Other Paid or Requested Distribution Outside USPS	1,417	1,417
4. Requested Copies Distributed by Other Mail Classes Through the USPS	0	0
c. Total Paid and/or Requested Circulation (Sum of 15b (1), (2), (3) and (4))	53,902	53,226
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3. Nonrequested Copies Distributed Through the USPS by Other Classes of Mail	0	0
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f. Total Distribution *(Sum of 15c and e)*	55,059	54,195
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h. Total *(Sum of 15f and g)*	55,857	55,728
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16. Publication of Statement of Ownership for a requester Publication is required and will be printed in the November 2008 issue of this publication.

17. Signature and Title of Editor, Publisher, Business Manager, or Owner:

Simon Young, Group Audience Marketing Director, September 23, 2008

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1. Publication Title: Test & Measurement World

	12 Month Average	September
Printed Circulation as reported on PS Form 3526, Line 15a	55,857	55,728
Digital Circulation	11,265	11,932
Total Circulation	67,122	67,660

Simon Young, Group Audience Marketing Director, September 23, 2008

dScope Series III
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RF instruments challenge PXI versatility

By Richard A. Quinnell, Contributing Technical Editor

One of the most dynamic applications for PXI is its use in the testing of complex, high-bandwidth RF applications. I recently spoke by phone with Tim Carey, PXI product manager at Aeroflex, who explained the difficulties of creating RF-capable instruments and who cautioned that multi-module RF instruments could limit PXI's versatility.

Q: How is RF a challenge for PXI?
A: Physical space is one of the main limitations that we have to work at overcoming. For one thing, the spacing of the boards makes it impossible for us to use double-sided component mounting and still provide shielding in a single-slot board. As a result, many RF instrument modules need two or more slots. Heat dissipation is also a challenge in such tight quarters. Also, the available rail voltages and currents, which are carry-overs from digital computing, are not what we would ideally like for RF.

Q: How is PXI providing an advantage?
A: The modularity of PXI allows us to separate the transducers from the processing capability of an RF instrument. CPUs evolve much faster than RF transducer technology, and the separation gives engineers access to higher-performance processors as soon as they become available. The separation also reduces the cost of upgrading. If a new processor or advanced transducer stage becomes available, engineers only need to change the system element that has improved rather than buying an entirely new instrument each time.

Q: What is the state of the art in PXI for RF?
A: Aeroflex and other vendors now offer modules that can produce and analyze signals with frequencies as high as 6 GHz, but we're beginning to see systems capable of operating at even higher frequencies. One signal analyzer now being demonstrated operates on signals to 26 GHz. Pretty good for a technology not intended for RF applications.

Q: What gaps do you see in the RF functionality available on PXI?
A: We haven't seen any real-time signal-generation capability for applications such as channel fading and base-station simulations. What is being offered now is the use of "canned" waveforms, not those computed in real time. PXI Express allows us to stream data through an RF module for complex, high-bandwidth signal generation, but some standards are best tested by having a closed loop and computing the test signal in real time.

Tim Carey
PXI product manager
Aeroflex

Q: Any concerns for the future?
A: If we're not careful, we may lose the versatility of the PXI architecture in RF instrument design. You have to break an instrument up into a number of functional blocks to put it on PXI. A signal analyzer, for instance, needs downconverter, signal-conditioning, and digitization blocks. But it is highly unlikely that vendors will do their partitioning the same way and have the same interface signals between blocks.

This will prevent engineers from creating instruments by combining modules from different vendors. The test system may be multivendor in nature, but not the individual instruments within the system.

Q: How can the industry avoid that?
A: The panacea would be for the industry to agree on the definitions of standard functional blocks and the interfaces between. Then engineers could mix and match vendor boards when creating their instruments. At the very least, though, there can also be collaboration between vendors to develop compatible blocks that will allow engineers to form instruments for themselves. □

INSIDE THIS REPORT

58 Guest commentary
58 Highlights
61 Chassis layout is key to success with PXI Express
64 Products

GUEST COMMENTARY

PXI changes how manufacturers deploy ATE

By Gary Clayton, MAC Panel Company

Experts involved in developing ATE (automated test equipment) applications cannot deny the revolution that has taken place since the introduction of the PXI platform. PXI, along with complementary software tools, now offers the opportunity to deploy functional test capabilities to electronics manufacturers in many more markets, yielding improved products and processes.

There are more than 1500 PXI instruments on the market, providing unprecedented configuration and performance possibilities. When coupled with software tools that simplify the process of integration, PXI-based ATE achieves ever-higher test coverage.

Test requirements vary by application and technology, but there are essential requirements common to all applications: comprehensive test coverage, ease of integration, and low initial and total life-cycle costs. I will focus here on ease of system integration and the associated positive impact on short- and long-term system costs.

The core elements that make up a typical functional ATE system include measurement instrumentation, signal switching, power sources, a software development environment, and a suitable electrical interface to bring the system resources to a single connection point for the unit under test—typically referred to as a mass interconnect. The ease with which a test system can be configured is largely governed by the instrument platform being used and the compatibility between the instrumentation and the available mass interconnects.

With the selection of instruments available for the PXI platform today, most system configurations can be housed in a PXI chassis, available in either a 3U or 6U form factor. By having all instrumentation and switching in one or more chassis, much of the rack size and system wiring associated with legacy platforms is eliminated. Mass-interconnect systems are offered in high-performance PCB (printed-circuit board) or traditional cable-connectivity formats.

Initial system configuration is just the start of the process. A good design will allow for future enhancements and upgrades. This is particularly true for the aerospace and defense markets, where system service will often exceed 20 years. The PXI platform has the resources and features necessary to make test system integration easy, robust, and reliable for the long haul. □

Gary Clayton is the director of sales and marketing at MAC Panel Company in Macclesfield, England. gpc@macpanel.com.

HIGHLIGHTS

Sundance debuts DSP/FPGA platform for PXI Express

In conjunction with becoming a member of the PXI Systems Alliance, Sundance Multiprocessor Technology has announced that it will introduce a range of PXIe (PXI Express) products for DSP (digital signal processor) and FPGA (field-programmable gate array) multiprocessor systems. Product roll out will begin with the SMT7 Series, which comprises more than 25 modular PXIe products.

The SMT702 provides eight PXIe lanes and two channels of 3-GHz analog-to-digital conversion that can be combined to deliver 6 Gsamples/s. It also features clock circuitry, two banks of DDR2 memory, and a Xilinx Virtex-5 FPGA optimized for logic and serial I/O.

The SMT700 carrier board will bring FPGA acceleration to PXIe systems. The board employs a Virtex-5 LXT or SXT device, which can be configured either through the onboard flash or through the Xilinx JTAG header. It includes a direct connection to an SLB (Sundance Local Bus) mezzanine card, enabling a variety of cards to be added to a system to provide Ethernet, video in/out, analog-to-digital conversion, and digital-to-analog conversion functions.

Data from these additional cards, along with data from the SMT700's own inputs—Gigabit Ethernet, 2.5-Gbps optical inks, and Rocket Serial Links—can be processed via the Virtex-5 or by another linked card or module. www.sundance.com.

Geotest to convert EADS tester to PXI

Geotest—Marvin Test Systems reports that it will implement the EADS Talon Instruments T964 series of digital test instruments in the PXI bus form factor. Currently, the T964, which is aimed at testing avionics and electronic equipment as well as communications products, is available in the larger VXI format.

James Mulato, president of EADS North America Test and Services, said, "Our T964 is the newest, most exciting test instrumentation product available in VXI and provides a comprehensive solution for testing today's advanced electronic boards and systems—as well as emulating older functional test systems and digital instrumentation." www.geotestinc.com; www.ts.eads-na.com.

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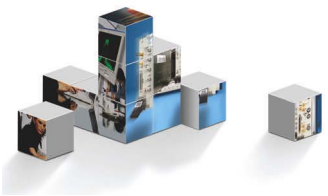

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Chassis layout is key to success with PXI Express

By Richard A. Quinnell, Contributing Technical Editor

With the electronics industry's never-ending appetite for speed, the bandwidth advantages of PXIe (PXI Express) are becoming increasingly important for test instrument designs. To take full advantage of the capabilities offered by this technology, you'll need a chassis designed to handle PXIe cards.

You could work with a manufacturer to design a custom card cage for your application, or you could turn to a commercial chassis offered by companies such as National Instruments (NI) and Geotest. Either way, you'll need to understand the connection architecture of the system backplane and then position the modules to maximize bandwidth usage.

Smaller PXIe enclosures such as the GX7600 offer hybrid slots that provide a growth path for PXI system developers. Courtesy of Geotest.

The place to start is by recognizing the fundamental characteristics of PCI Express, the serial bus that provides PXIe its bandwidth. PCI Express provides system elements with a point-to-point serial connection composed of multiple lanes, each of which has both send and receive channels operating at 2.5 Gbps. Designers can scale the performance of PCI Express connections to meet performance needs by grouping lanes together; configurations of x1, x4, x8, and x16 lanes are common. Because the lanes run point-to-point, their data bandwidth is dedicated to the connection, not shared with other connections in the system.

Compatibility is key

A key component of the PCI Express bus is its compatibility with traditional PCI. Anything that can connect to the PCI bus can connect through a bridge chip to a PCI Express bus without any software changes. The bridge chip handles all the mapping of transactions across a shared parallel bus onto a dedicated serial bus. This software compatibility ensures that PCI and PCI Express elements can work together in a system as though they were all on the PCI bus.

When adapting PCI Express for the PXIe specifications, the PXI Systems Alliance (PXISA) sought to take advantage of this ability to interoperate in order to help developers preserve their investment in PXI modules. The PXIe specification calls for the PXIe system controller to communicate with PXIe modules as well as through a bridge to a standard PCI-based PXI bus. In addition, the specification defines a hybrid module slot that accepts either PXI or PXIe modules. These two definitions ensure that developers can mix traditional PXI and new PXIe modules in the same system without software changes.

The specification does not, however, define how many of each type of module slot—PXI, PXIe, or hybrid—a system enclosure must contain, nor does it specify the arrangement of slots beyond the locations for the system controller and system timing module. These choices are left open for developers to make as needed, and many custom configurations are thus possible. In their commercial PXIe system enclosures, Geotest and NI have already made those choices for you, but you still need to pay attention to how you position your modules to make the most efficient use of bandwidth.

Small cages ease development

Geotest offers a nine-slot hybrid PXIe enclosure, the GX7600, that provides five PXI slots, two hybrid slots, a PXIe controller slot, and a PXIe system timing slot. The backplane supports a x4 lane connection from the system controller to each hybrid slot as well as the system timing slot. It also has a x1 lane connection to a bridge chip that drives the five PXI slots. NI has a similar, eight-slot enclosure, the NI PXIe-1062Q, that offers only four PXI slots but otherwise offers the same connections as the GX7600.

The relative simplicity of these small enclosures means that there is only one positioning issue to keep in mind. The hybrid slots replace the PXI J2 connector that carries a PXI local bus with a different connector to carry the PXIe bus. PXI cards that use the local bus and J2 connector thus cannot be located in a hybrid slot.

Modules that do not have a J2 connector, however, can be positioned anywhere in the chassis, which makes these chassis good candidates for developers who are just beginning to need the PXIe bandwidth or who see PXIe needs looming but not yet present. The hybrid slots provide a growth path for eventual adoption of PXIe: You can use PXI modules for the present design and then replace them with higher-performance PXIe modules without having to change software or modify the system configuration. *(continued)*

Positioning modules in larger PXIe chassis

In addition to its small hybrid enclosures, NI has introduced two 18-slot PXIe enclosures: The NI PXIe-1065 provides a PXIe system controller slot, four hybrid slots, four PXIe slots (including the system timing controller), and nine PXI slots; the NI PXIe-1075 has no pure PXI slots, offering one controller, nine PXIe, and eight hybrid slots.

Connections for the 18-slot enclosures are somewhat more complex than for the smaller configurations. The NI PXIe-1065 breaks the PXI bus into two segments. One contains five PXI slots and a hybrid slot while the other contains four PXI slots and three hybrids.

The first segment has a x1 direct link to the system controller, while the second shares a switched x4 link to the controller with two PXIe slots. The NI PCIe-1075 uses four switches on its backplane. This organizes the hybrid slots into two four-slot PXI segments and the PXIe slots into two additional groups, each collection sharing a x4 link to the controller.

Even developers with no current need for PXI Express can benefit from properly positioned cards in a PXI Express cage because of the split PXI bus that enclosures such as the NI PXIe-1065 offer.
Courtesy of National Instruments.

This type of grouping and use of switches creates pathway restrictions that impact the data bandwidth and inter-module connectivity available at any given slot. The way you position modules in a PXIe enclosure, therefore, can affect the data throughput of a system. For instance, the presence of two independent PXI buses in the 18-slot cage allows you to bypass a bottleneck when two groupings of PXI modules require high bandwidth in order to transfer data back and forth. If all the modules are located on a single segment, the groups must share the PXI bus. If the two groups are located on different segments, each grouping has sole access to its segment's bandwidth.

Because the links from the segments to the system controller are also independent, the effect is like having two small independent systems that share common clock and

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trigger functions. The enclosure thus offers a system performance boost to developers not using PXIe at all.

Switches offer opportunities

When positioning modules in the PXIe slots, developers should pay attention to the location and nature of the switches on the backplane. In the PXIe-1075, for instance, each switch serves to connect the system controller and four or five other connections using x4 links to the PXIe slots or a x1 link to the PXI bridge. These switches force the PXIe modules that connect to them to share the link bandwidth. You will get maximum performance, therefore, if you use separate switches to isolate high-demand module groupings from one another.

You should be aware that the PXIe links in the cages currently available from NI and Geotest are limited to x4 configurations. Yet, some high-performance PXIe modules offer x8 connections to achieve maximum performance. The specifications allow the system controller to provide up to 24 PCI Express lanes configured as a x16 link and a x8 link or as multiple clusters of fewer lanes with the same total. Thus, the PXIe specification supports the x8 connections of such modules, but the currently available commercial backplanes do not. To gain this top performance, you will need custom backplanes for your enclosures.

When creating custom backplanes, you will need to partition the available links while bearing in mind how data flows within the system. Fortunately, you have a wide range of options for developing dedicated and shared-bandwidth connections. Switches, for instance, provide a means of distributing one link from the system controller slot to multiple module slots. The slots will have to share the bandwidth of the link to the controller, but they may not need to share bandwidth for connections among them. Nonblocking switches can provide independent pathways among ports, so two ports can link together and not share bandwidth with a similar linking between two other ports on the same switch.

The key, however, is to recognize the opportunities as well as the restrictions that a specific PXIe backplane configuration offers. An ad hoc insertion of modules into the enclosure can create performance obstacles. By positioning modules within the enclosure appropriately, however, you can maximize the performance attainable, making the most out of PXI Express. □

PRODUCTS

Pickering introduces high-current switches

Pickering Interfaces has expanded its range of PXI high-current switching products with the introduction of a family of high-power solid-state relays. The range comprises eight modules configured as fault-insertion, SPST (single-pole, single-throw) relay, multiplexer, and matrix switches capable of handling 10 A at 200 V and 30 A at 40 V. Each unit occupies two slots in a 3U chassis.

The 40-192 is a six-channel fault-insertion switch with two fault buses capable of hot-switching signals up to 10 A and 200 V. The 40-191 uses the same architecture, but is capable of switching signals of 30 A and 40 V and handling surge currents in excess of 120 A with no lifetime degradation. Each module can simulate most common faults found in a system, including open circuits and short circuits to one of two fault connections.

The other models in the family are the 40-182 and 40-183 six-channel SPST solid-state relay switches; the 40-666 and 40-667 solid-state multiplexers, which are available in dual three-channel or single six-channel configurations; and the 40-553 and 40-554 6X2 solid-state matrices.

Pickering Interfaces, www.pickeringtest.com.

Adlink debuts 19-slot PXI chassis

The PXIS-2719 from Adlink Technology is a RoHS-compliant 3U 19-slot PXI chassis that provides one system controller slot and 18 peripheral card slots. It also provides uniform air flow for each slot with a maximum 10% difference in temperature measured on load boards during testing. The fans pull cool air in from the bottom of the chassis, through the PXI modules, and then exhaust it out the rear. This design minimizes hot air draw from the rear of the rack where all other devices typically exhaust.

Through a feature the company calls "smart chassis management," fan speed is controlled either automatically based on the internal temperature or manually through user input. Chassis temperature, fan speed, and system voltages are self-monitored to ensure system stability. The PXIS-2719 also supports remote management by providing chassis status through an RS-232 connection. An optional rack-mount kit allows the chassis to be recessed up to 10 cm in a cabinet rack to accommodate multiple wires and connectors or mass-interconnect modules.

Adlink Technology, www.adlinktech.com.

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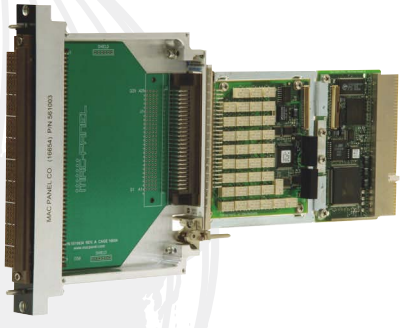

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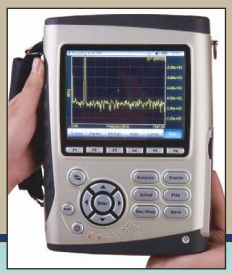

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VIEWPOINT

[An exclusive interview with a technical leader]

JUSTIN TESTA
Executive VP
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In 2008, Justin Testa was named executive VP and group business manager of the Cognex Modular Vision Systems Division, with responsibility for strategic planning and product development in four major areas: vision systems, vision software, vision sensors, and ID products. Testa joined Cognex in 1983 as a sales engineer and has held a variety of positions including senior VP of marketing, where he was responsible for worldwide product management, marketing communications, industry and competitive analyses, and new business development. He holds a BA from Boston University and an MBA from Boston College.

Contributing editor Larry Maloney interviewed Testa at the Cognex offices on trends in machine-vision technology.

Vision market hinges on ease of use

Q: What will it take to get the machine-vision industry out of its slump?

A: Recovery depends in part on improvements in the general economy, especially in semiconductors, electronics, and automotive—all vital markets for machine vision. But those factors aside, our challenge as an industry is to find ways to solve more problems for customers. If we want to grow the market, we must address their pain and the burning need for new solutions. That's why Cognex invests heavily in R&D even during downturns.

Q: What are the chief improvements that customers want to see in vision systems?

A: Ease of use is always a concern. We need to make it easier not only to create a vision application but also to deploy and maintain an application. In my view, the machine-vision market is more "ease-of-use elastic" than it is "price elastic."

Q: Which of the vision applications targeted by Cognex is growing the fastest?

A: Hands down, the fastest growing application is industrial identification. In fact, the company's very first product back in 1982 was an optical character reader for industrial part tracking. It started with wafer tracking in the semiconductor field but has broadened over time to embrace the need of many industries for cradle-to-grave traceability of parts and products.

Concurrent with that has been the rise of many enabling technologies, such as the 2-D symbol and direct part marking. We now sell a family of DataMan ID readers, which incorporate our powerful machine-vision capabilities, into many markets, ranging from automotive and electronics to medical devices and pharmaceuticals. In cases of recalls, being able to trace a part to a particular lot number through ID can save a company enormous expense.

Q: What application ranks next in terms of growth?

A: That would be the broad area of inspection, which embraces many applications, such as presence/absence, dimensional checking, and defect detection. Opportunities in defect detection, for example, are opening up as a result of higher-resolution cameras and faster image processing.

Q: What are the chief applications for your new In-Sight Micro Vision system?

A: It packs a complete general-purpose vision system into a small package about the size of a remote-head camera. Measuring just 30x30x60 mm, the system is paired with our new EasyBuilder configuration software and VisionView operator interface display.

The result is a more affordable and accessible vision system for all sorts of automation, especially in embedded applications where space is at a premium. For example, you'll see In-Sight Micro integrated into automation devices, such as the end effectors on robots.

Q: Looking ahead, what are some of the emerging applications for machine vision?

A: One area that is getting more interest is 3-D imaging, which could certainly help grow the vision market. We are putting more investment into color vision systems, and we see that area growing as well. More opportunities in defect inspection should also open up, with better resolution cameras, improved lighting, and more powerful processors. In many of these applications, continued progress in putting more intelligence into vision-software tools will hold the key to success. T&MW

Justin Testa addresses more questions on vision hardware and software technology in the online version of this interview: www.tmworld.com/2008_11.

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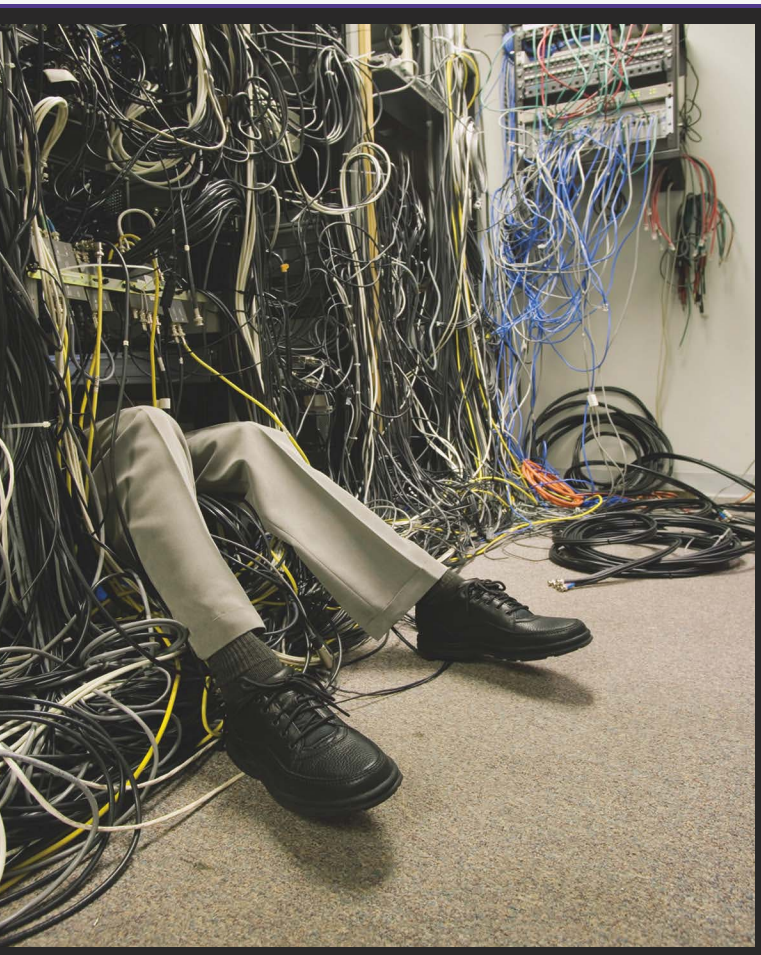

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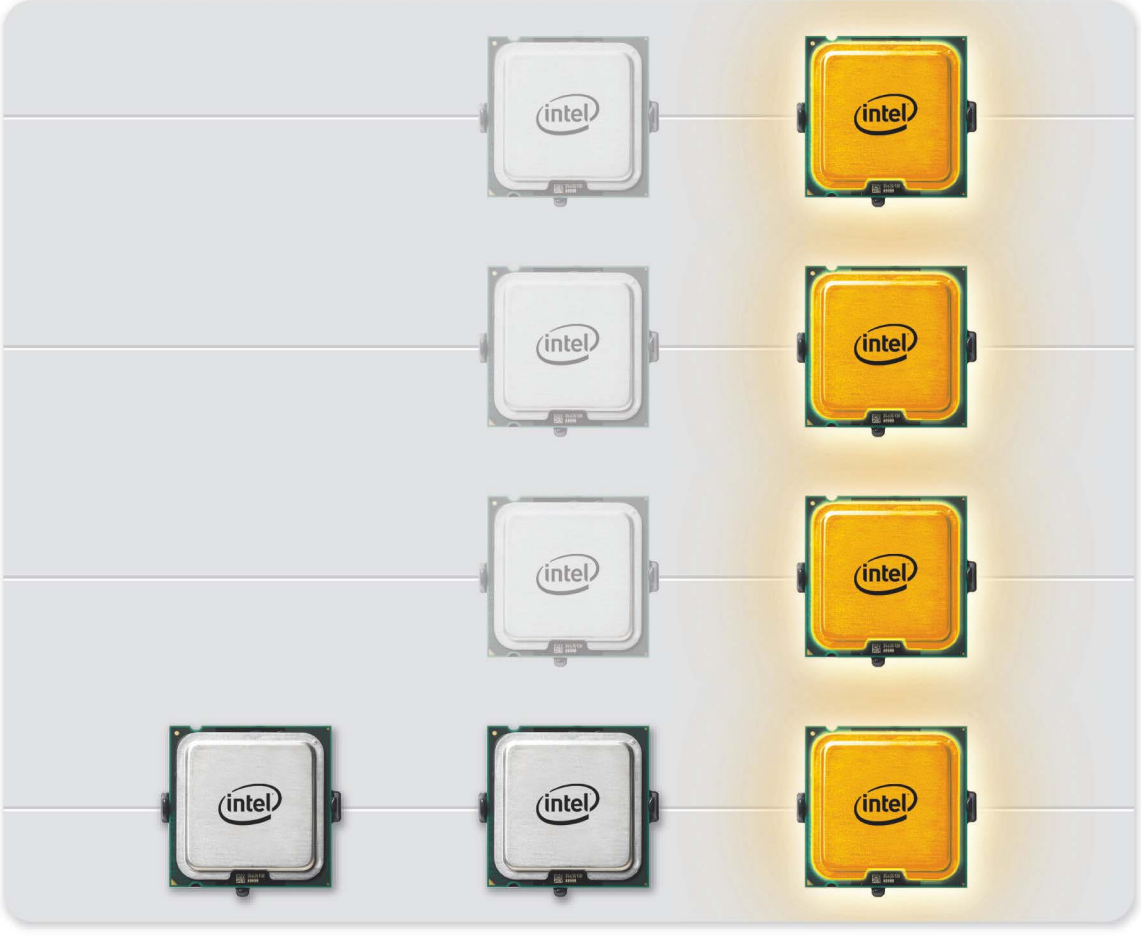

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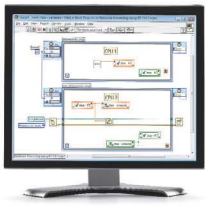

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